# DESIGN, SYNTHESIS AND APPLICATION OF REVERSIBLE LOGIC ARCHITECTURES FOR ENERGY AWARE SUSTAINABLE COMPUTING

**A Thesis Submitted**
**In Partial Fulfillment of the Requirements for the Degree of**

## DOCTOR OF PHILOSOPHY
## in
## COMPUTER SCIENCE AND ENGINEERING

**by**


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**FACULTY OF ENGINEERING AND TECHNOLOGY**
**MAHARISHI UNIVERSITY OF INFORMATION TECHNOLOGY,**
**LUCKNOW,**

**JANUARY-2023**

# Candidate's Declaration

I hereby declare that the work presented in this thesis entitled **DESIGN, SYNTHESIS AND APPLICATION OF REVERSIBLE LOGIC ARCHITECTURES FOR ENERGY AWARE SUSTAINABLE COMPUTING.** in fulfillment of the requirements for the award of Degree of Doctor of Philosophy submitted in School of Engineering &Technology , Maharishi University of Information Technology, Lucknow is an authentic record of my own research work carried out under the supervision of **Dr. Santosh Kumar** (**Associate Professor**) , **Department of Computer Engineering & Information Technology** in this University. I also declare that the work embodied in the present thesis

i) Is my original work and has not been copied from any journal/ thesis/ book; and
ii) Has not been submitted by me for any other Degree or Diploma of any University/ Institution.

Date -

( Nirupama Pathak)
Enrollment No. : **MUIT0118190002**
Research Scholar

# CERTIFICATE

It has been confirmed that Nirupma Pathak (MUIT0118190002) has carried out the research presented in this thesis entitled "**DESIGN, SYNTHESIS AND APPLICATION OF REVERSIBLELOGIC ARCHITECTURES FOR ENERGY AWARE SUSTAINABLE COMPUTING**" under my supervision at Maharishi University of Information Technology, Lucknow. The contents of the thesis do not constitute the basis for the award of any other degree to the candidate or to anyone else from this or any other University/Institution.

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**Assoc. Prof.,**

**CE and IT**

**MAHARISHI UNIVERSITY OF INFORMATION TECHNOLOGY, LUCKNOW,**

Date: 01-01-2023

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# List of Symbols and Abbreviations

| Symbol/Abbreviation | Representation/Explanation |
|---|---|
| VLSI | Very large-scale integration |
| NoT | number of transistors |
| GDI | Gate diffusion input |
| CMOS | Complementary metal oxide semiconductor |
| mv | minority voter |
| F2G | Feynman double gate |
| R-CQCA | Reversible-Conservative quantum-cellular- automata |
| CNOT | controlled NOT gate |
| TG | Toffoli Gate |
| FRG | Fredkin Gate |
| GC | Gate count |
| GO | Garbage output |
| QC | Quantum cost |
| UD | Unit delay |
| RAM | Random access memory |
| QCA | Quantum dot cellular automata |
| CAM | Content-addressable memory |
| NML | Nanomagnetic Logic |
| pNML | Perpendicular nano-magnetic Logic |
| iNML | in-plane nano-magnetic Logic |
| PMA | perpendicular magnetic anisotropy |
| MAJ | Majority Gate |
| R/W | Read/Write |
| EDA | Electronic design automation |
| ALU | Arithmetic logic unit: |
| PG | Parity Generator |
| PC | Parity Checker |
| VH | Very high |
| NI | No improvement |
| PG\ PC | Parity generator\ parity checker |
| Ex-OR | Exclusive OR |

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# DESIGN, SYNTHESIS AND APPLICATION OF REVERSIBLE LOGIC ARCHITECTURES FOR ENERGY-AWARE SUSTAINABLE COMPUTING

**Nirupma Pathak**
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## ABSTRACT

With the spectacular rise of processing speed and high-density circuits, the design of low power based architecture has sparked enormous attention. Traditional digital circuit design is based on irreversible computing, which further reduces processing speed and results in substantial energy consumption. Technology such as reversible logic based nano-circuits, which employ qubit based computing, have been developed as a solution for next-generation computing circuit applications and energy-conscious circuits, with a focus on high-speed computing and low energy dissipation. Reversible computing-based circuit technology reboots the input logic depending on the output node for backward calculation.

As part of this dissertation effort, the reversible conservative multiplexer circuit is synthesised, which is the first contribution. A substantial amount of literature work in reversible computing-based multiplexer circuits has been created, however, the optimal multiplexer circuit has not been presented. However, in the literature, a conservative logic-based multiplexer circuit for testing purposes has been introduced. To verify the design of a conservative reversible multiplexer in a physical environment, QCA technology is employed. This suggested conservative reversible multiplexer has been improved in terms of reversible parameters.

CAM memory are the essential components that are utilised as cache memory and match logic units in very high-speed search calculations that may be completed in a single clock cycle, or parallel. The design of an efficient CAM memory architecture is the subject of this dissertation's second chapter. The suggested CAM cell design has two blocks, which are referred to as the memory and the matching unit. Additional to this, both the blocks memory and the matching unit have been implemented in QCA and pNMLtechnology to fully meet the requirements of the high-speed nano-electronics computing application.

The following are some of the unique contributions in this dissertation work:

**i** A cost-effective conservative reversible multiplexer circuit is introduced that meets the requirements of the quantum world, such as a low value of quantum cost, ancilla input, and a unit delay. It is shown that the suggested conservative reversible multiplexer circuit can be constructed in QCA technology and that is compared to the current work design costs, such as cell count and latency, and found that reduced parameters, when compared to the current work, and the suggested conservative reversible multiplexer circuit outperforms it.

**ii** A modular design algorithm for a conservative reversible m:1 multiplexer is presented, as is a method for implementing the algorithm.

**iii** A new idea based on molecular-QCA and pNML technology is presented in the form of a synthesis of the CAM memory system. Additional comparisons with existing circuits demonstrated a significant improvement in practically all parameters when compared to the current circuits. To compare the current state of a QCA measure to a previous state, all primary QCA measures are employed, including the total number of cells, number of majority gates, latency (number of clock cycles), and area. Measurements such as bound box area and clock cycle delay are taken into account in the pNML technology to compare the proposed CAM structure. Based on our comparison results, the recommended form of CAM memory as stated is more likely to meet the criteria of an optimal circuit for nano-computing applications, as seen in the figure cost is one of the important parameters.

**iv** Digital circuits based on the pNML technology for use in nanoelectronics applications, including the parity generator and checker, as well as the ALU for robust design is introduced. The objective is to develop a framework for optimising pNML designs to employ a less number of magnets while yet being flexible enough to be used in complex system designs in the future. Following the completion of this synthesis, the new design is suitable for use in the fabrication of nano-electronics circuits. The MagCAD tool was used to check the digital circuits in the synthesised designs before they were implemented. In this work, the major purpose is to construct a robust ALU design in terms of bounded box area and other cost primitives. When comparing the outcomes of these studies. It was found that the use of unique digital designs produces superior results and results in a more robust architecture when compared to the literature works.

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First and foremost, I would want to express my profound gratitude to Dr. Santosh Kumar. I couldn't have asked for a better supervisor than the one I have now. Working with and with Dr. Santosh Kumar was a fascinating and rewarding experience. I'm grateful to have had the opportunity to work with someone of this calibre.

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**(Nirupma Pathak)**

**MUIT, Lucknow**

# CHAPTER 1

## INTRODUCTION

The approach of scaling in MOS transistors is confined due to physical limits in device performance and manufacturing as per Sadhu et. al [1], which makes it difficult to use. Because of its fast processing speed and low power consumption, it is an excellent choice. digital logic circuits based on dynamic logic and fewer transistors play an essential role in current computer systems as per Khan et. al [2]. One possible option may be quantum-dot cellular automata (QCA) technology, which is based on nano-computing. As a result of its high packing density, high-speed nano-technology approach, and promisingly decreased power consumption during computing, this QCA technology is a viable choice for nano-circuit fabrication and has the potential to replace traditional MOS technology as per Roy et. al. [3]. QCA technology is being utilized to develop low-power circuits and to reduce power consumption in nano-circuit applications, which is a significant step forward. The ultimate objective is to construct nano-circuits using QCA technology in Gaussoumi et. al [4]. QCA is an emerging nano-technology approach for manufacturing circuits at the nano-scale level as per Wang et. al. [5]. QCA based circuit synthesizes with very low power consumption, high computation, and high complexity in a compact chip footprint.

Miniaturization in the direction of high computation in VLSI is a difficult element to overcome for next-generation products. The core of non-magnetic technology must be understandable to the creators of developing technologies in Riente et. al. [6]. Digital circuits need increased processing speed while simultaneously decreasing circuit complexity and power consumption in Sai et. al. [7]. Nano-magnetic logic (NML) is an emerging technology that implements such an architecture at the nano-scale and therefore appears as a potential alternative to the CMOS-VLSI architecture in Breitkreutz et.al. [8]. As the scaling of logic circuits continues to reduce, there is an increasing demand for alternative technologies to fill the gap. NML is a viable alternative that has piqued the curiosity of a large number of academics and researchers as per Cofano et.al [9]. The reduction of circuit density and speed is driving the development of new research parameters for high-speed logic designs. A new nano-technology approach based on nano-magnetic logic circuits has been created, and it is described here. As a result, this technology has the possibility of combining logic computation with storage in the same device, indicating that it has significant potential for use in new technologies in Pala et. al. [10]. Because NML technology is fast nearing its lowest feature size, highest device density, and ability to operate at room temperature, it is becoming more popular as per Breitkreutz et. al. [11]. NML based devices that use less power, integrated devices with high device density, and minimal leakage are all important characteristics of the NML technology as per Bhoi et.al. [12]. A nano-magnetic tool was developed by ToPoliNano (TOrinoPOLLItecnico Nanotechnology) names as MagCAD as per Riente et. al. [6]. For this study, NML technology is separated into two categories: in-plane NML (iNML) and perpendicular NML (pNML). Magnetic anisotropy serves as a criterion for distinguishing

between these two categories. The advantage of using an NML-based logic circuit is that it consumes very little power and can be used at room temperature as per Causapruno et.al. [13]. The classification of iNML and pNML is based on the direction of the magnetic field. It is referred to as iNML if the magnetic orientation is in-plane; however, it is referred to as pNML if the magnetic orientation is perpendicular to the plan in Riente et. al. [14]. The pNML category of the NML family is more efficient in terms of having a smaller footprint area and using much less power.

## MOTIVATION

The shrinking of the MOS transistor becomes a key task at a given stage in the production process. QCA technology is a new nano-scale alternative that is gaining popularity as per Kamrani et. Al. [15]. In nano-technology, QCA is focused on high speed and low power consumption in computing, making it a feasible alternative to CMOS technology. QCA is a revolutionary computer technology that offers advantages such as lower power consumption and faster processing speed as per Seyedi et. al. [16].

As scaling down advances at a rapid pace, the need for an alternate semiconductor device to replace standard CMOS technology develops. Because of its high device density and fast processing speed, NML has received a great deal of interest among the alternatives. NML technology is distinguished by its low-power processing, high device density integration, and zero leakage, among other characteristics as per Gypens et. al. [17]. It is necessary to understand how perpendicular nano-magnetic logic (pNML) works to build circuits that function as digital logic. CMOS technology is being phased out in favour of NML-based digital logic devices, which are becoming more common as per Mattela et. al. [18] All of the distinguishing characteristics of reversible logic, QCA, and NML technologies encourage the development of a nanocircuit based on emerging technology in the domain of nano-computing.

## OBJECTIVE

Making a multiplexer is a complicated task, and thinking about the structure and architecture of the design in the context of reversible logic involves requires a significant amount of paper effort. Existing research efforts on reversible multiplexer architectures are missing in rigour and comprehensiveness, and this has to be addressed. According to previous research, the proposed reversible multiplexer has a lower overhead in terms of quantum cost when compared to the existing work.

Making CAM memory in QCA and pNML technologies is a very tough undertaking. The proposed CAM architecture is compared to various earlier studies on CAM memory, and the findings show that our approach outperforms existing techniques in terms of design parameter overhead for a wide range of test circuit types. The proposed CAM memory as compared to relatively recent research, and it was determined that the proposed work was better in every way. Circuit designs such as a reversible multiplexer and CAM memory in the QCA method are recommended for use in the era of nano-computing since they are cost-effective and provide a benefit.

The suggested pNML-based ALU architecture is very robust in terms of latency and area, and it is also highly efficient. It has been determined that the ALU layout design in pNML

technology is the most suitable for creating efficient circuits. Comparing the results of this study to earlier work, the researchers discovered a significant decrease in the pNML parameters in terms of latency and area for several benchmark samples. Through the use of a variety of methodologies, this thesis proposes an efficient digital circuit architecture that strives to bridge the gap between architectural reality and design completeness.

## METHODOLOGIES OF THE RESEARCH

Presented in this dissertation work is an advanced architecture consisting of reversible multiplexers, CAM memory, parity generators, parity checkers, and arithmetic logic units (ALUs), all of which are physically implemented. Each one of the suggested architectures is distinct and cost-effective so that it is suitable for energy-aware sustainable computing.

Steps that are followed during the research are described below:

- Gaining an understanding of the reversible R-CQCA gate and using this conservative reversible gate to synthesize and conservative reversible multiplexers design.
- Understanding the memory and match logic block and with this blocks synthesis the CAM memory block.
- The half adder, OR, Ex-NOR, AND multiplexers are all represented in the pNML layout; understanding this arrangement, and designing the pNML layout of the ALU is the next step.

## THESIS ORGANIZATION

This section provides a high-level summary of the dissertation. A foundational section of the dissertation is provided to assist readers in comprehending the terms used throughout the dissertation. As part of determining the superiority considerations for the planned research, the associated state-of-the-artwork, as well as its issues and limitations, is examined. This dissertation is split into five chapters, each of which is labelled with the numbers 1 through 5.

### Chapter 1

The essential notion of this dissertation work is discussed in Chapter 1. The overview of this dissertation work are included a short explanation of motivation, aim, methodology, work outline, and thesis arrangement.

### Chapter 2

The second chapter provides a basic review of several technologies such as GDI-CMOS, reversible logic, quantum computing, QCA, and pNML.

### Chapter 3

This chapter covers the synthesis technique, simulation results, and design parameters for the conservative reversible multiplexer.

### Chapter 4

The design technique for content addressable memory based on QCA and pNML technologies are discussed in this chapter.

**Chapter 5**

Using nano-magnetic logic technology, Chapter 5 comprises different digital logic circuits such as parity generators, parity checkers, multiplexer and ALUs.

## 1.4 CONCLUSION

This chapter, after presenting reversible logic, quantum technology, QCA and pNML technology, as well as their methodology of the work. A detailed description of the structure of this thesis is also provided.

# CHAPTER 2

# FUNDAMENTAL AND STATE-OF-ART-WORK

## FUNDAMENTAL OF GDI, REVERSIBILITY CONCEPT, QUANTUM TECHNOLOGY, QCA AND NANOMAGNETIC TECHNOLOGY

In today's nano-electronics system design, one of the fundamental problems is to create a cost-efficient product, while also using less power in Shahidi,et. al. [19]. However, the best possible power value is achieved without sacrificing speed, area, or high-performance applications in the process. This is geared at the use of modern technologies. This is to say that, the next generation of nano-electronics applications in quantum technology represents a completely novel technology as per Pallav et. al. [20]. Power dissipation correlated to heat dissipation is a critical restriction of electronic equipment. Overheating, information loss, and, in certain situations, component failure is all consequences of power loss in electronic systems in Dmitri et.al. [21]. The transistor count in integrated circuits is doubled every two years, according to Moore's law of exponential growth. The amount of power needed by a device is directly proportional to the amount of heat lost by that device, and the greater the number of components a device has, the more power it needs in Gerhard et. al. [22]. The higher device density used by the device means it greater the amount of heat dissipated. In other words, if the power expended by a device is more than the power required by the device's design, the heat created will not be able to be quickly dispersed, resulting in overheating. Overheating may cause component failure and, in the worst-case scenario, partial or complete failure of the device in Adriano et. al. [23]. In electronic systems, a reduction in the amount of heat dissipated by the system provides an advantage in terms of high densities and speeds while maintaining no loss of information in Jurcevic et.al. [24]. Since the early 1990s, several low-power approaches have been developed and used to overcome the limitations of CMOS semiconductor technology. For this reason, various quantum nanotechnologies have evolved in which quantum gates are widely accessible in Kwon et. al. [25].

As per famous R. Landauer’s principle [26] drawn that logically irreversible systems, which erasure of a logic-bit is always associated with a high value of the entropy. For the system to function properly during calculation, all of the erased logic bits in the system must dissipate about kTln2 of heat, where k is Boltzmann's constant and T is the absolute temperature at which the process is carried out. To be reversible, Bennett [27] the principal, has determined that an energy-free computing system is required C.H.Bennett et. al. Quantum Computing uses the concept of “Quantum mechanics” of superposition and entanglement through quantum gates, which are reversible both physically and logically, thereby reducing loss of power in electrical systems in Hevia et. al. [28]. This chapter deals a fundamental of some of the fundamental details about GDI, reversible computing, QCA computing, quantum computing and nano-magnetic logic.

### Basics of GDI-CMOS Technique

Gate diffusion input (GDI) based cell consists of two transistors of type P-MOS and N-MOS and is almost similar to the CMOS inverter as shown in Fig 2.1. A GDI cell contains three inputs, which are denoted by the letters G, P, and N, as per Ponnian et.al. [29]. Input G means gate, which is associated with both NMOS and PMOS type transistors. The P is an input signal, which can either be the source/drain of the PMOS transistor. The N is input-signal which can either be the drain/source of NMOS transistor.

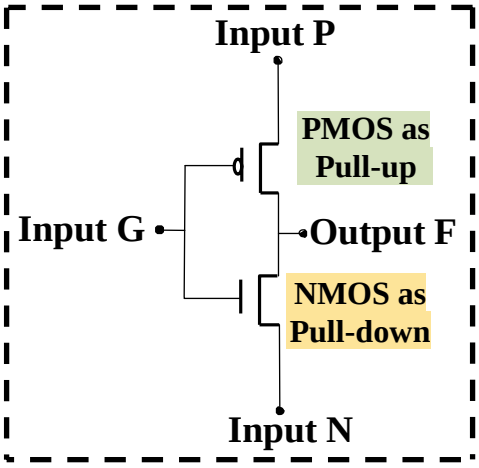



**Fig. 2.1** Schematic of basic GDI-CMOS based gate

Both PMOS and N-MOS type transistor bulks are connected to nodes N and P respectively. The input nodes, P and N can be biased random depending on the function of the cell. The main dissimilarity between the CMOS inverter and the GDI basic cell is that in the CMOS inverter, the P-MOS drain is associated with the input-power and the N-MOS source is grounded while that in GDI cell, the inputs, G, P and N can be given to power supply or can be grounded or taken as input depending on the function of the circuit. This effectively decreases the number of transistors for implementing basic logic circuits and different complex functions compared to its CMOS implementation.

### Implementation of Different Functions using GDI-CMOS Technique

GDI-CMOS is a very fundamental cell because of its simplicity and ability to generate basic logic operations like AND, OR, MUX, inverter, and XOR as per Krishna et.al. [30]. The three input GDI cell based on PMOS and NMOS transistor is shown in Fig 2.1. It can be seen that the GDI cell consists of three inputs nodes like K, L and M at nodes G, P and N, respectively. By setting the configuration of the input nodes as Gate (G), P diffusion (P) and N diffusion (N) in the GDI cell, various logical operations can be performed as shown in Table 2.1. The output logic is dependent on the input node values in the GDI cells of the inputs. Table 2.1 presents the logic operation based on a GDI cell by setting inputs. Many functions can be realized using the GDI technique by changing nodes G, N and P inputs of GDI cell given in Table 2.1 accordingly while using fewer transistors compared to CMOS implementation. GDI cell has three nodes G, P and N and node inputs are denoted as K, L and M respectively.

**Table 2.1.** Generating of basic operations using the GDI cell

| Operation of GDI cell | No of transistors | Node G | Node P | Node N |
|---|---|---|---|---|
| OR logic | 2 | K | L | High |
| AND logic | 2 | K | Low | M |
| MUX logic | 2 | K | L | M |
| NOT logic | 2 | K | High | Low |
| XOR logic | 4 | K | L | L |

Note: K means-input at node G, L means-input at node P, M means-input at node N, High means-DC Supply VDD, Low means-Ground Gnd

### Comparison between GDI-CMOS and conventional CMOS logic gates transistors

Fig 2.2, shows a comparison of the number of transistors (NoT) needed for the various logic functions created using the GDI approach and CMOS technology. NoT is reduced using the GDI technique for different logic functions compared to that of CMOS logic gates as per Krishna et. al. [30]. The above basic GDI-CMOS logic gates are used for building any logic circuits.

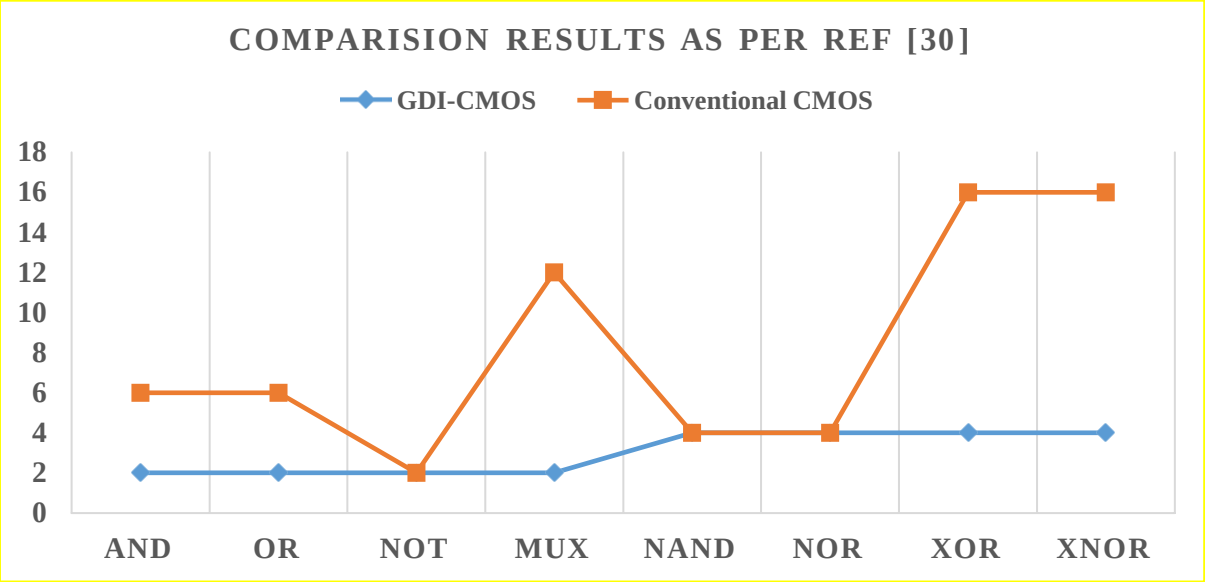



**Fig.2.2** NoT needed for GDI-CMOS and conventional CMOS based logic technique

### Fundamentals of Reversible Computing

Using the notion of "Second law of Thermodynamics," reversibility is shown in nature. This law asserts that if any system is reversible, then the entropy of that system remains constant. When the entropy of a system remains constant, no heat is dissipated in the system as per Singh et.al. [31]. For a system to be reversible, it must be in a state of equilibrium. Consequently, if the reversible principle is applied to the circuit design, there will be no heat dissipation, resulting in no power loss in the system as per Gaur et. al. [32]. It is necessary to design at two major subsystem levels when developing a reversible digital electronic system, namely the gate level designing and the transistor level designing. All of the components of a digital electronic system, including the logic and physical hardware, should be reversible. As a result, the reversibility notion must be implemented at both the gate and transistor levels to

create energy-efficient, recyclable digital systems or circuits that do not produce heat or lose information as per Saeedi et.al. [33].

**Definition 2.1.** It is necessary to have an equal number of inputs $I_v(A_0, A_1,...A_n)$ and outputs $O_v(B_0, B_1,...B_n)$, as well as the bijective mapping, as illustrated in Fig. 2.3 (a) of the reversible gate.

**Definition 2.2** A conservative, reversible gate is defined as one in which the hamming weight of the inputs and outputs is equal, as seen in Fig 2.3 (b). A more acceptable representation would be in the form of an equation (2.1).

$$A_1 \oplus A_2 \oplus .....A_n \xleftrightarrow{\text{bijective}} B_1 \oplus B_2 \oplus .....B_n \qquad (2.1)$$

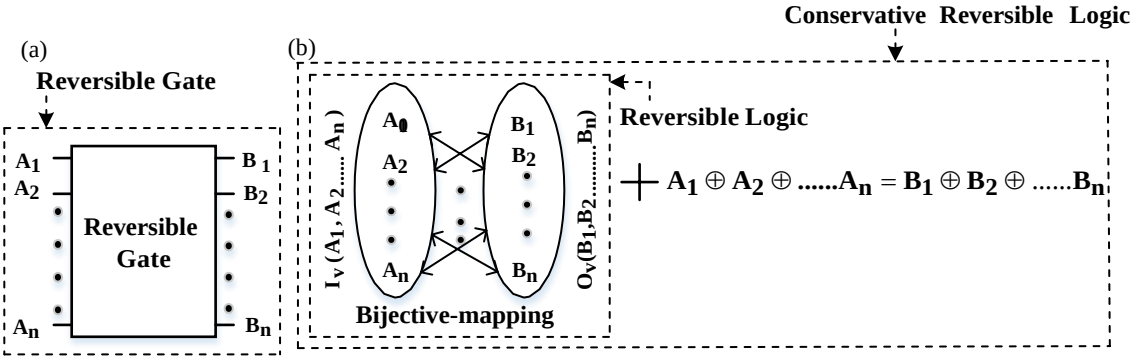



**Fig. 2.3** An n x n architecture of (a) reversible gate (b) conservative reversible gate.

**Definition 2.3.** The significant cost-metric parameter for reversible logic is quantum cost. Any reversible gate can be decomposed into 1 x 1 and 2 x 2 gates such as CNOT, V and $V^+$ gates (called quantum primitive gates).

The CNOT gate is depicted in Fig. 2.4 (a) and the quantum cost calculation for some basic structures are depicted in Figs. 2.4 (b), 2.4 (c), 2.4 (d), 2.4 (e). The cost is calculated by counting total primitives gates. The controlled V and $V^+$ gates are depicted in Fig. 2.4 (f). In the controlled V gate when the control input A=1, implies Q=V(B), that V is synthesized by equation 2.2. When A=0, implies Q=B, where A and B are inputs and Q is the output. The V and $V^+$ gates have some basic properties that are drawn in equations (2.3) and (2.4).

The quantum cost parameter is a cost-metric parameter that is important for reversible logic. Any reversible gate, such as the CNOT, V, and V+ gates, can be divided down into two types of quantum gates: 1 x 1 and 2 x 2 gates (called quantum primitive gates) as per Große et.al. [35]. The CNOT gate is depicted in Fig. 2.4 (a) and the quantum cost calculation for some basic structures are depicted in Figs. 2.4 (b), 2.4 (c), 2.4 (d), 2.4 (e). The cost is computed by adding up the entire number of primitive gates. The controlled V and V+ gates are shown in Fig. 2.4 (f). When the control input A=1, which means Q=V(B), the V gate is synthesised by equation 2.2 in the controlled V configuration. When A=0, Q=B is implied, where A and B are the inputs and Q is the output of the equation. The V and V+ gates have several fundamental qualities that are shown in equation (2.3), as well as in equation (2.4).

$$V = \frac{i+1}{2}\begin{pmatrix} 1 & -i \\ -i & -1 \end{pmatrix} \qquad (2.2)$$

$V \times V = V^{+} \times V^{+} = NOT$ (2.3)

$V^{+} \times V = V \times V^{+} = I$ (2.4)

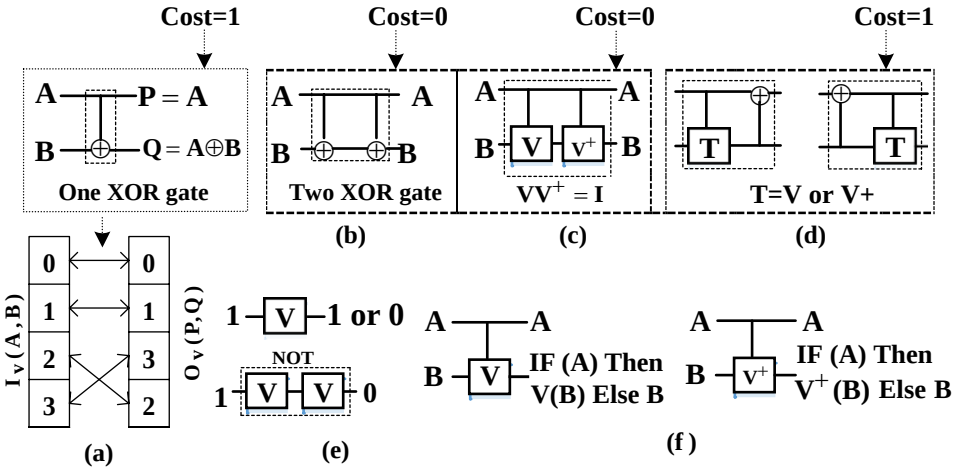



**Fig. 2.4** Basic of Quantum cost

### Logical-Reversibility

The number of outputs on reversible logic gates is the same as the number of inputs. When it comes to reversible logic gates, there is an equal number of one-to-one mappings between input vectors and output vectors, which means that inputs can be recovered using outputs and the reverse is true. Except for the NOT gate, no other logic gate is reversible. Reversible gates get balanced functions at the outputs if inputs don't have any constants as per Jamal et. al. [35]. If some of the inputs of reversible gates have constants, then outputs can have unbalanced functions with extra inputs and garbage outputs (outputs that are not important for the execution of the function) depending on the functionality of reversible gates. Several novel reversible logic gates have been introduced by researchers since the last decade. Some of the basic reversible logic gates are TG, FG, and FRG gates to use the reversible gate based quantum circuit design as per Jamal et. al. [35].

### Physical-Reversibility

Physical reversibility is achieved by making design reversible. If any system at the device level doesn't have any energy loss while running the system backwards, then the system is said to be physically reversible. To achieve physical reversibility, adiabatic logic is applied to CMOS circuits. The adiabatic circuit gives stored energy or RC across the load capacitance back to the Power clock's purpose is to not turn "transistor on" when voltage is across it and not turn "transistor off" when current is flowing through it. If we maintain the above conditions in all phases in the slow movement, then the restore phase will recover energy back to the power clock. This helps in restoring energy without loss when the system or circuit run backwards. Using Reversible logic gates and applying adiabatic logic to any CMOS circuit can help in reducing power and heat. But adiabatic CMOS circuits have disadvantages because of slow speed and high area overhead. Technologies such as QCA, Magnetic spin devices, adiabatic CMOS, and nano-magnetic (pNML or iNML) have succeeded in quantum computing technology for physical reversibility. The many steps of digital hardware are shown in the flow chart shown in Fig. 2.5; the logical reversibility is presented in the fifth level, and the physical reversibility is presented in the sixth level, respectively as per Sridharan et. al. [36].

## Quantum Technology and Quantum gates

Logic computations, sensing, imaging, and simulations are all made possible by quantum technology, which is a promising developing technology that makes use of the notion of quantum physics. Quantum technology is the application of quantum physics ideas like tunnelling, entanglement, and superposition.

In quantum computing, quantum circuits are constructed using quantum gates, which are reversible and operate on "qubits," which are small units of information. Qubits are used in quantum computing for retracing information because they are entangled (sealed) when they enter a quantum gate and they preserve their entangle when they come out of a quantum gate as per Fredkin et. al. [40]. Quantum gates are reversible devices that allow for the retracing and restoration of information. A unitary matrix may be used to represent quantum gates to simplify their representation. In a quantum gate, the input qubits and the output qubits are the same as one another. In contrast to classical gate states, which may only be either 0 or 1, quantum gate states or vectors are referred to as "kets," and they can be either 0 or 1. In the matrix form shown below, a single qubit "p" has two probability kets or vectors associated with it.

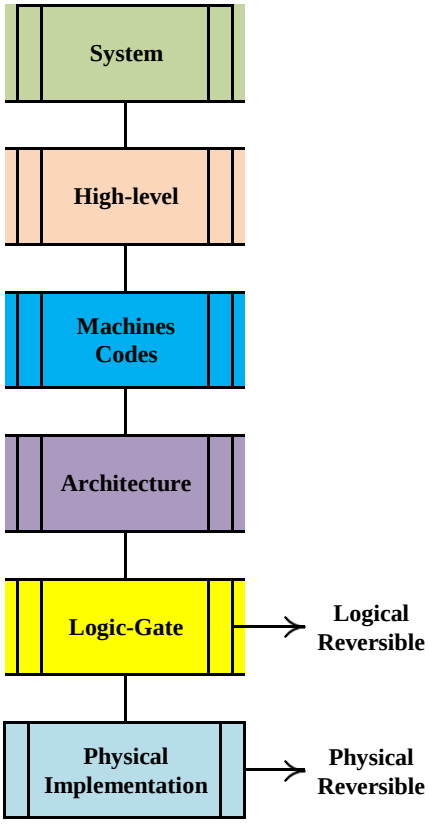



**Fig. 2.5** Logical and Physical reversible approach in the digital hardware system

$$|p\rangle = \begin{matrix} V_0 \\ [V_1] \end{matrix}$$

Here, ket for "0" value $|0\rangle = \begin{matrix} 1 \\ [0] \end{matrix}$ and ket for "1" value $|1\rangle = \begin{matrix} 0 \\ [1] \end{matrix}$

Similarly, two qubits “p and q” have four vectors in a matrix given below.

$$|pq\rangle = \begin{matrix} V_{00} \\ V_{01} \\ [V_{10}] \\ V_{11} \end{matrix}$$

The quantum gates can process complex information computations securely without loss at high speeds with low power compared to CMOS reversible gates, but has more scope for error, making the quantum gate designing the complex. Quantum technology readily offers reversibility, security and highly complex and sensitive computations. There is a lot more to be researched in the future to build an efficient error-free quantum circuit as quantum technology has reduced energy dissipation compared to conventional CMOS technology.

**Fundamentals of QCA Technology**

The scaling approach in MOS transistors has several limitations, and it is now experiencing restrictions because of channel length restrictions associated with nano-technology manufacturing problems and other factors Angizi et. al. [41]. With the progress of technology and improvements, power dissipation has become a critical restriction, which has a negative impact on the performance of portable devices as per Lent et.al. [42]. The use of device power has a significant impact on the performance of portal devices such as mobile phones, sensors, medical equipment, and battery life Pal et. al. [43]. As a result, the device size, weight, and cost of portable systems are restricted. To attain high-performance devices, the clock frequency must be raised, and to deal with the extra heat, a cooling circuit must be included, which in turn increases density to limit power consumption and minimise heat created. The use of QCA technology has been suggested as a potential alternative as per Sasamal et.al. [44].

The QCA technology is a well-known nano-technology that uses majority gates to create logic circuits rather than transistors, so achieving the status of a transistor-less technology as per Misra et.al [45]. A number of its appealing characteristics, including low density, low-power- consumption, fast computing speed, and high scaling over CMOS technology, distinguish it as a future trend technology that may be utilised to construct electronic devices with nano-scale dimensions Teja et. al [46].

The power-dissipation, short channel effects, and quantum effects challenges that CMOS technology is encountering in respect to chip size are preventing it from being able to integrate additional transistors before approaching its scaling constraints as per Askari et. al. [47]. Many new technologies have arisen in recent years to overcome this issue, which is referred to as 'Beyond CMOS Technologies,' and to continue the trend as per Ashima et.al [48]. These technologies are described as follows: QCA is a newly developed nano-technology that provides a solution to the scaling limitations of the CMOS technology. QCA is a kind of majority gate based logic circuit. Because of its characteristics, the QCA technology is widely utilised for the efficient design and implementation of digital circuits. The polarisation of the QCA cell can only be accomplished in one of two methods. As seen in Fig. 2.6, the polarization of the QCA cell is -1 and +1, respectively as per Syamala et.al. [49]. Following is a diagram illustrating the binary states of QCA cells that exist depending on the polarisation of the cells. The most significant building elements of QCA are QCA wire, inverter, majority type gates, AND, OR gates, and they are shown in Fig 2.7. Making one of the inputs of the majority gate low or high, respectively, may be used to provide operations such as AND, OR logic gates.

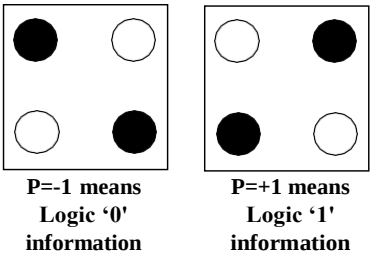



**Fig. 2.6** Basic QCA Cell ($90^0$cell)

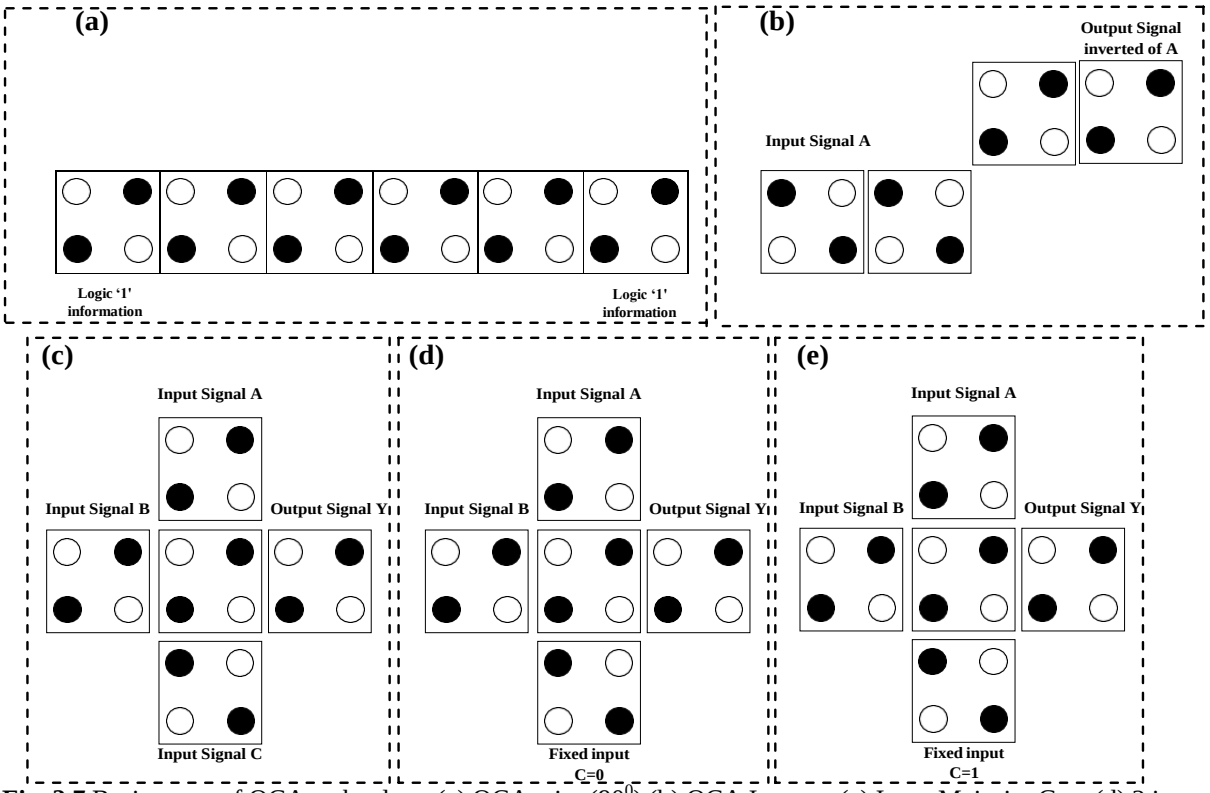



**Fig. 2.7** Basic types of QCA technology (a) QCA wire ($90^0$) (b) QCA Inverter (c) Input Majority Gate (d) 2 input QCA AND Gate realized using 3- input Majority Gate (e) Input QCA OR Gate realized using 3 inputs Majority Gate

. Quantum cells (also known as quantum dots) are the fundamental computing units of QCA technology. Each cell includes four quantum dots in each of its four corners in Syamala et al. [49]. Each quantum cell is used by two electrons, both of which can tunnel mechanically through the lower potential barrier between the four dots in the quantum cell. Fig 2.8 (a) depicts the wire type pattern created by a quantum cell in the current instance. When designing QCA wire, the repeating manner of cell placement near to each other is taken into consideration. The QCA wire is made up of cascading cells that are used to transport bits from one node to another. Fig 2.8 (a) illustrates two different QCA structure arrangements that are based on rotation, such as the $45^0$ and $90^0$ configurations. In QCA layout, the NOT (Inverter) and majority gate are one of the most common. In QCA Design, the majority voter gate is treated as a rudimentary building component. The architectural outlooks for the inverter are shown in Fig 2.8 (b), where one architecture has a greater cell count than the other architecture, which is in contrast to the new architecture of the inverter (which has a lower cell count). During the first kind of inverter, the inputs are separated into two distinct directions, and after that, the inputs are combined by a cell with $45^0$ rotation, which results in the inverter polarisation. MV (3-inputs) = ABC+BC+AC and MV (5-inputs) = ABC+ABD+ABE+ACD+ACE+ADE+BCD+BDE+CDE are the basic blocks in QCA layout that decide the Boolean expression of majority voter gate, and it is a particularly valuable gate because of its excellent characteristics in synthesising elementary logic functions such as OR, AND gates. As seen in Fig. 2.8 (c), the 3-input majority voter gate is used, and it should be noted that in the outer cell, one cell polarisation 1 or 0 is fixed to produce the OR, AND logic calculation, while in the inner cell, one cell polarisation 1 or 0 is fixed to generate the OR, AND logic computation. The MV gate is composed of 5 numbers of cells, with the outer three cells serving as the input. Fig 2.8 (d) shows a 5-input Majority voter gate with a single output. The single design depicted in Fig. 2.8 (e) depicts the construction of synchronised input-based AND, OR gates. The unsynchronized input caused by erroneous clocking framing in the circuit creation of AND, OR gates is shown in Fig. 2.8 (f) in yet another architectural design. Data transport between nodes in QCA is accomplished via the use of clock pulses, which are the most essential unit in the system as per Sen et. al [50]. Within the QCA framework, the clock pulse has two fundamental functions: the first is to give sufficient energy to the design, and the second is to convey data from source to destination. The flow of electrons inside the quantum cell is enabled by a four-phase clock, which also provides adequate energy to various paths in the cell. The four-phase clocks are all programmed to run in the same sequential sequence as one another. As seen in Fig. 2.9, the majority of four-phase clock systems are divided into four segments, which are labelled switch (S), hold (H), release (R), and relax (Rex). Initially, the concept of cell polarisation is introduced at the switch mode and continues until the maximum polarization is obtained. The hold mode is the most advanced stage of the clock-pulse extents, and it occurs when the cell holds the highest amount of polarisation. When the cell clock allows it, the polarization of the cell decays, which is referred to as the release mode. Finally, when the cell is in relax mode, it is no longer polarised.

**Definition 2.4**. In QCA, each cell comprises a quantum dot that contains four quantum dots. Quantum dots have a circular shape with a predefined diameter of 10nm, and each dot is spaced 20nm apart from its closest neighbour. Regardless of whether two more electrons are inserted in two quantum dots that already exist, the arrangement will always be in a diagonal direction unless. The QCA cell that has been produced may have a distinct polarisation (Fig. 2.6 (a)). Polarization may be used to specify the binary value that is stored in the QCA cell. Equation 2.5 is used to represent the polarisation expression.

$$P = \frac{(\sigma_1 + \sigma_3) - (\sigma_2 + \sigma_4)}{\sigma_1 + \sigma_2 + \sigma_3 + \sigma_4} \qquad (2.5)$$

**Definition 2.5.** It is the utility's responsibility to govern the flow of information across QCA's four clock zones. Four clock zones are separated into four phase groups, which are divided into four clock zones (Switch, Hold, release and relax) as per Sen et. al. [50]. Fig.2.9 depicts the time zone on a clock.

**Definition 2.6.** When the maximum and lowest energies are dissimilar, the kink energy is calculated. The largest amount of energy is created when the two cells have opposing polarisation, and the least amount of energy is created when they have the same polarization. Equation 2.6 is used to calculate the kink energy. As shown in equation 2.7, the electrostatic energy of a circuit is created by considering two cells (named Cell A and Cell B) with differing polarizations (named $P_a$ and $P_b$) placed next to each other in a circuit.

$$E_{kink} = E^{m,n}_{P_m \neq P_n} - E^{m,n}_{P_m = P_n} \qquad (2.6)$$

$$E_{m,n} = \frac{1}{4\pi\varepsilon_0} \Sigma_{k=1}^{4} \Sigma_{l=1}^{4} \frac{q_k^m q_l^n}{|r_k^m - r_l^n|} \qquad (2.7)$$

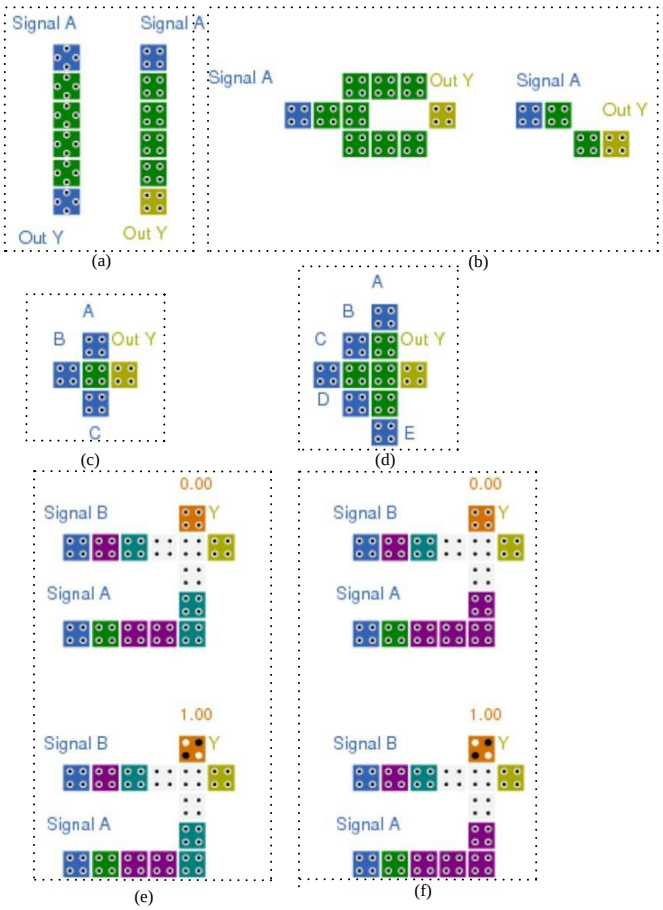



**Fig. 2.8** A component of QCA (a) Rotation based $45^0$ and $90^0$ wires (b) Inverter (c) 3-input Majority Gate (d) 5-input majority gate (e) Synchronized AND, OR gate (f) Unsynchronized AND, OR gate.

Electrons are repelled and attracted due to coulombs interaction. Coulombs law is given by equation 2.8.

$$F = (k)\frac{q_1 q_2}{r^2} \qquad (2.8)$$

Where,

F is the force between two charges $q_1$ and $q_2$

K is the coulombs constant,

$q_1$ and $q_2$ are charged,

The distance between two charges, $q_1$ and $q_2$, is represented by the symbol r.

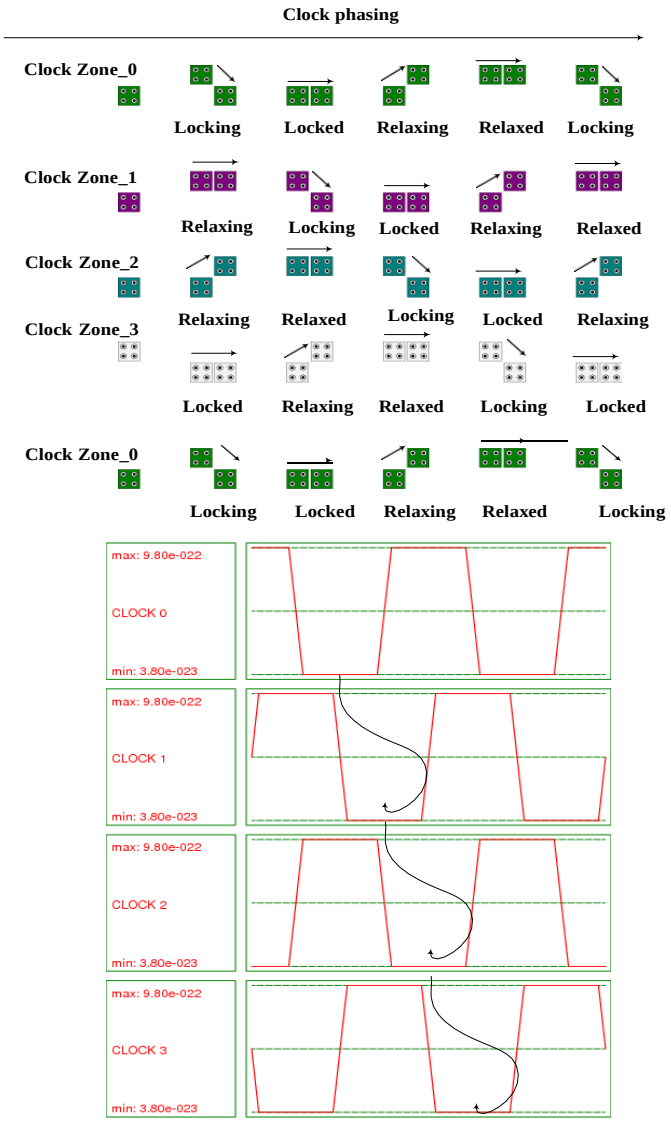



**Fig. 2.9** Four-phase clock in QCA

According to Coulomb's law, the attraction and repulsion of charges are dictated by the distance between them, as well as the sign and magnitude of the charges involved in the interaction. Whenever the signs of the two charges are in opposition to each other, the force

is negative (attraction force). When both charges have the same sign, the force is positive (repulsion force). Electrons have a negative charge in a nucleus, while holes have a positive charge in the same structure. Unlike other electrons, electrons are attracted to holes and are repelled by them.

**Fundamentals of Nano-magnetic Logic**

According to Moore's law, the size of devices is reducing to the point that twice as many transistors can be packed on a single chip every eighteen months, or every two years, and the size of devices continues to diminish. Beyond a certain scaling limit, CMOS is hitting its technical and economic boundaries, and it has certain drawbacks such as its physical size, power consumption, leakage current, higher fabrication costs, and short channel effect as per Angizi et.al. [41]. As a result, researchers have developed a new configuration in which information processing is based on magnetism, in which interacting sub-micrometre magnets are used to perform logic operations and propagate information at room temperature as per Pal et.al. [43], and in which information processing is based on magnetism is performed at room temperature. Nano-magnetic logic is the term used to describe this technique (NML). It is not necessary to use transistors to execute magnetic operations at the nano-scale for these technologies to work. Logic information is encoded into the magnetization direction by elements acting as nano-magnets, and this information is sent to the nearby magnet via the dipole field coupling of the elements as per Pala et.al. [10]. Scalability, non-volatility of stored information, immunity to radiofrequency radiation, no leakage current, and the consumption of very little power are the primary benefits of nano-magnets as per Causapruno et. al. [13]. It decreases the number of wires in the circuit, and as a result, it solves the issues associated with signal routing. At room temperature, it is possible to readily produce nano-magnets as per Riente et.al. [14]. Using nano-magnetic logic, it is possible to integrate memory and digital-logic circuits on the same device, although at different levels. Based on their magnetic orientation, nano-magnetic logic may be split into two categories: in-plane nonmagnetic logic (iNML) and perpendicular nano-magnetic logic (pNML). When the magnetic orientation is in-plane, the magnetic orientation is referred to as iNML, and when the magnetic orientation is perpendicular to the plane, the magnetic orientation is referred to as pNML. In iNML has a few drawbacks, such as a restricted number of cascaded components, which necessitates the use of more than one clock pulse. A significant advantage of pNML technology is that it has excellent inherent physical qualities, and just a single clock pulse is needed for the system as per Breitkreutz et.al. [11], making the circuit more compact and straightforward to construct. The domain wall conductors, which were employed for signal routing, were adopted by the monolithic 3D circuit. To assure accurate calculation of pNML, shown that time-dependent nucleation in field-based linked nano-magnets may be achieved by field-based coupling. It has been discovered that when the wire ends are constructed triangularly pointed as opposed to rectangularly pointed in as per Breitkreutz et.al. [11], the domain nucleation field can be controlled with perpendicular magnetic anisotropy, and a 60 percent decrease in switching field may be detected. The minority voter and the inverter are the basic modules of pNML technology. In this section, the pNML technologies are demonstrated that was employed in this dissertation.

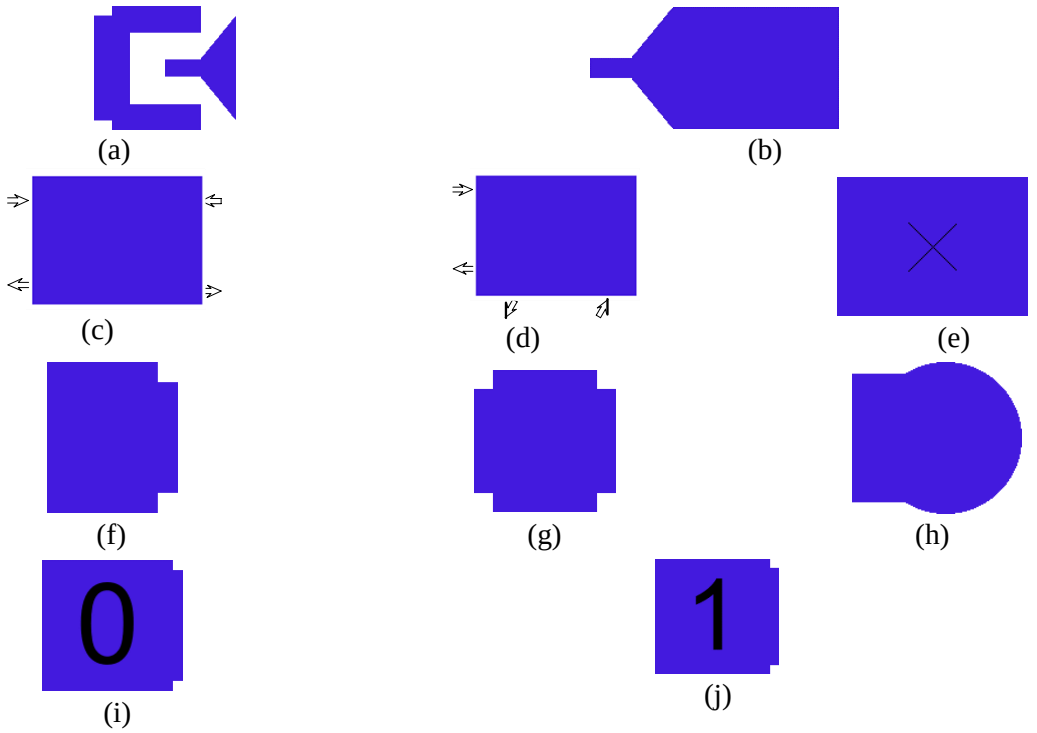



**Fig. 2.10** Elements of pNML (a) inverter magnet (b) artificial nucleation center (c) Domain wall magnet (d) corner magnet (e) via magnet (f) t magnet (g) x connection magnet (h) pad magnet (i) fixed '0' (j) fixed '1'

A representation of the pNML architecture of an inverter magnet is shown in Fig. 2.10 (a). It is possible to separate the critical routes by using an inverter to invert the input signal and split the critical paths as per Bhoi et.al. [12]. It is important to note that the input type magnet is linked to the output type magnet in the inverter architecture. Fig. 2.10 (b) depicts an artificial nucleation centre (ANC), which is a form of output magnet with a magnetic field. Fig 2.10 (c) illustrates how in pNML, the point-to-point connection is made possible via magnet wires, also known as 'domain wall' magnets, which are connected. Fig. 2.10 (d) depicts a corner magnet, which is utilised to generate output with a $90^0$-degree rotational axis. Fig. 2.10 (e) depicts the 'via magnet,' which is utilised to link to a nucleation centre that is located on an adjacent plane to form a crystal. To divide the input into two separate directions, as seen in Fig. 2.10 (f) 't shaped' magnet is utilised. As seen in Fig. 2.10 (g), the 'x-shaped' magnet is utilised to divide the input signal into three separate directions. As shown in Fig. 2.10 (h), a 'pad magnet' is employed to bring the magnetic wire to a complete stop. When it comes to the output, pads serve as a nucleation centre. To construct a certain logic gate, fixed '0' and fixed '1' inputs are necessary. Figs. 2.10 (i) and (j) show examples of fixed input in pNML technology with a fixed value of '0' and a fixed value of '1.'

### Architecture of Minority voter gate

The inputs of the minority voter (mv) gate are linked to the nucleation centre, and the output (Y) is connected to the pad magnet in this configuration. The output will provide the lowest possible value of the A, B, and C logic values. The inputs A, B, and output (Y) of the mv gate are all located on the same layer, however, the input C is located on a separate layer in the architecture of the device. As seen in Fig. 2.11, two separate layers are taken into consideration for correct magnetization between the magnets, which is three-dimensional. When input A is set to '0', the mv gate is handled as a NAND gate, and when input A is fixed to '1', the mv gate is treated as a NOR gate, respectively. Table 2.1 shows the truth table for the

mv gate, which corresponds to the truth table for the mv gate. With an odd number of inputs, the ANC is an mv gate that can be configured to have as few as one and as many as five. The nucleation centre is impacted by the superposition of coupling of odd inputs, and the outputs are influenced by the clock signal and the inputs they are coupled to. This design, which is represented in Fig. 2.11, includes a nucleation centre, a majority function get, and a final output inversion in addition to the majority function get in Fig. 2.11 (b).

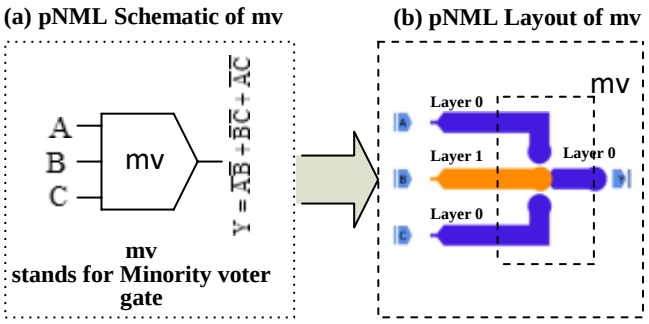



**Fig. 2.11** Minority voter gate schematic and layout

Table. 2.2 The truth table of minority voter gate

| Inputs | | | Output | Remark |
|---|---|---|---|---|
| A | B | C | Y | |
| 0 | 0 | 0 | 1 | Fix input A=0, mv as NAND gate |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 1 | |
| 0 | 1 | 1 | 0 | |
| 1 | 0 | 0 | 1 | Fix input A=1, mv as NOR gate |
| 1 | 0 | 1 | 0 | |
| 1 | 1 | 0 | 0 | |
| 1 | 1 | 1 | 0 | |

## STATE-OF-THE-ART WORK

In this section, the existing work on the reversible multiplexer, CAM memory, parity generator and ALU has been studied. Multiplexer, CAM memory and ALU have played a major role in synthesizing the microprocessor, and processor architecture as Per et.al. [43]. QCA and NML technology are a possible alternative that has sparked a lot of interest among researchers. Nano-technology-based QCA and NML offer a lot of advantages, including high device density, rapid processing, and low latency. Researchers are striving to discover the most efficient design characteristics, such as less cell count and less area. The increasing study field in the nano-electronics domain is a necessary precondition for the assessment of synthesis, optimization, and verification. A great number of publications have been published in the literature on the synthesis of nano-electronic circuits using QCA, reversible logic, and pNML technology, among other techniques as per Askari et.al. [47], Chabi et.al. [37], Sen et.al.[38]. The current status of this field's study shows that a large amount of the works that focus on the nano-circuit are based on QCA and pNML framework, but few works consider as optimised design.

The 2:1 multiplexer circuit by the authors in Thapliyal et. al. [39] was introduced by the conservative MX-cqca gate, however, it is non-reversible. There are certain limitations to this multiplexer circuit, such as the fact that the modular method cannot be improved for higher-order multiplexers and that the quantum circuit cannot be achieved since it is non-reversible.

In Vankamamidi, et. al. [51], the design of a one-bit memory cell in QCA technology was carried out in both line-wise based memory cells and loop-wise based memory cells, with the latter being the more common. When compared to the line-wise based memory cell, the loop wise memory cell has a major disadvantage in that it is difficult to design and requires more clock schemes or zones, which increases the delay Frost et.al. [52], whereas the loop wise memory cell is simple to design and does not require more clock schemes or zones because feedback is used in this type of memory cell, which was studied in Taskin et.al. [53], Ottavi et.al. [54]. Digital circuits based on QCA technology were developed in Satyanarayana et.al [55], Foroutan et. al. [56] for the types of combinational such as an even parity generator, multiplexer and ALU circuit.

## CONTRIBUTION TO THE CONTEXT OF THE DISSERTATION

As a result, following a thorough review of the literature works on this reversible logic, quantum technology, QCA, and pNML technologies, it was discovered that the limitations of the majority of these works were focused on circuit synthesis and optimising metrics while lacking optimal parameter values. This dissertation work represents the culmination of previous efforts to address the limitations of earlier works.

The optimization of circuit synthesis is accomplished via the use of circuit design. The proposed circuits have been constructed and confirmed using the QCADesigner and pNML tool, respectively. The results of the simulation show that the system is operating as intended. Furthermore, when compared to previous research, the performance of the suggested circuits is shown to be improved in terms of parameters, as presented here.

# CHAPTER 3

# CONSERVATIVE REVERSIBLE LOGIC BASED MULTIPLEXER CIRCUITS

In the nano-scale size range, there are many fundamental limits to CMOS circuit design, including MOS transistor width (W), length (L), and the short channel effect, all of which contribute to a reduction in device performance as per Singh et.al [31]. To solve these difficulties, researchers turned to nano-technology as per Sridharan et.al. [36]. Recently discovered QCA general theorems offer the concept of low power consumption, high device density, fast switching speed, and high operational frequency (THz) as per Chabi et.al [37]. Reversible logic, on the other hand, is a prominent topic in the field of quantum technology, since it is capable of doing computation with almost little power usage as per Sen et.al [38]. The reversible logic approach is becoming more popular in low-power applications such as nano-electronics and quantum computing. Particularly concerning quantum circuits, they are of nano-metric size and have a high calculation speed. Because they utilise very small particles (known as qubits) and exist at the atomic scale level, they are considered to be quantum computing as per Sen et.al [38]. The benefit of reversible logic is that it is used in quantum computing, which is a new technology. Furthermore, reversible logic is a top-level new technology that processes high-speed computing while using little power and operating on a nano-metric scale in Angizi et.al [41], Jamal et.al. [35]]. Conservative-based circuits are developed with a concentration on fault management, which improves the dependability of the circuits as a result. The second most essential issue is the cost, which is the most fundamental component of the quantum cost. Concentrating on these two factors will result in a significant improvement in the overall efficiency of the circuit. The originality of this work lies in the fact that it designs circuits by incorporating all of the two aspects mentioned above.

## RELATED WORK ON CONSERVATIVE MULTIPLEXER CIRCUITS

Multiplexer circuits are the most essential component of all digital integrated circuits, and they are contained in the module section of the control unit of the processor's control unit. The multiplexer serves as the control unit of the processor, which is more suitable as per Jamal et.al [35]. Following a review of the state-of-the-art work in this area, it can be concluded that

a significant amount of research has been done in this domain, except for a few works that focus on the conservative approach, combined quantum logic circuit, and QCA framework as per Sen et.al [38], Teja et.al [46], Askari et.al [47], Malhotra et.al. [48], Syamala et.al [49], Sen et.al [50]. While the authors in Sen et.al [38] provide a 2:1 multiplexer circuit but it is not optimize. There are certain limitations to this multiplexer circuit, such as the fact that the modular method cannot be improved for higher-order multiplexers and that the quantum circuit cannot be achieved since it is non-reversible. When all of the existing research is taken into consideration, it can be concluded that our suggested circuits contain certain unique characteristics, such as low-cost metric parameters (gate count, garbage outputs, and quantum cost). In the more particular multiplexer, the design method was expanded to accommodate n-bit input utilising the algorithm that was devised. The suggested multiplexer has been implemented in a QCA architecture that is suited for the present nano-electronics confinement application, which has been developed further.

## CONTRIBUTION TOWARDS THE DESIGN OF MULTIPLEXER CIRCUITS

This chapter proposes a conservative reversible multiplexer with minimal quantum cost that is based on quantum computation. The following are the general contours of the workaround circuits that have been suggested.

- A conservative, reversible m:1 type multiplexer based on the R-CQCA gate is suggested, which has been implemented using QCA technology. When compared to current quantum circuits, the provided quantum circuit demonstrates that it is more cost-effective in terms of quantum cost and unit delay.
- The robust layout of the multiplexer is presented in QCA technology. The results of the simulation describe the right functionality for the shortest possible clock cycle delay.

## THE PROPOSED MULTIPLEXER BASED ON NEW REVERSIBLE GATE

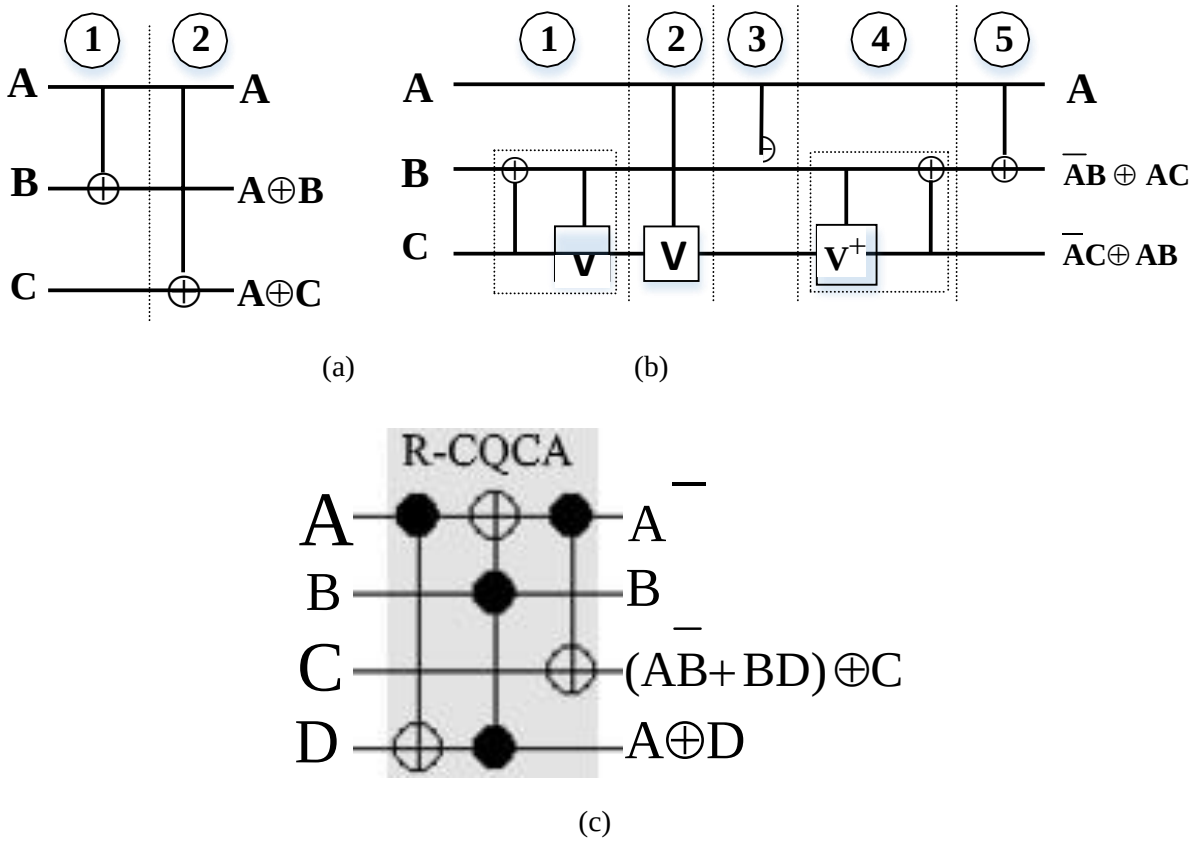
The conservative logic claims to have a cost-efficient use in reversible logic circuits, which may be used to test the circuit. According to Misra et.al [45], the conservative characteristic is a key aspect of the process of evaluating reversible gates. The conservative and reversible approach, as a result, would be regarded as a valuable characteristic for the design of circuits because of its ability to achieve a low error rate and testing capability. The proposed conservative, reversible logic is implemented in the QCA approach and it meets cost-effective concerns such as decreasing cell complexity, reducing delay, and reducing layout space as per Sen et.al [50].

It has been shown that an existing reversible gate may be used to design a new multiplexer circuit as per Misra et.al. [45]. It is necessary to use the R-CQCA gate for the multiplexer circuit. Multiplexer circuits are discussed in detail in Section 3.3.2.

### Existing conservative, reversible gates

F2G and FRG are two of the most popular conservative, reversible gates currently available. In F2G input vector is $I_V$ the output vector $O_V$ and they are set by $I_V(A,B,C)$ and $O_V = (A, A \oplus B, A \oplus C)$. In FRG input and output vectors are set as $I_V(A,B,C)$ and

$O_v = (A, A\overline{B} + AC, A\overline{C} + AB)$ . One of the other conservative, reversible gates is the R-CQCA; it is popular owing to the low value of quantum cost as per Misra et.al [45]. The quantum costs of F2G, FRG, and R-CQCA are 2, 5, and 6, correspondingly. The R-CQCA gate, which is conservative and reversible, is employed to synthesise the multiplexer in this study. F2G, FRG, and R-CQCA quantum equivalent circuits are shown in Figs. 3.1 (a), 3.1 (b), and 3.1 (c), respectively, as quantum equivalent circuits.




(a) (b)

(c)

**Fig. 3.1** Quantum Circuit of (a) F2G (b) FRG (c) R-CQCA

**Modular approaches to design a multiplexer**

Specifically, in the computational area, the multiplexer is utilised to pick the specific data set as per Jamal et.al [35]. 1x R-CQCA is used in the construction of the 2:1 Mux design, and its unit delay is one. The 2:1 mux, as represented in Fig. 3.2 (a). The 2:1 mux is made up of one select line (Sel), two input information lines ($I_0$ and $I_1$), and one needed output line (Out). The output is synthesized by $Out = \overline{Sel}(I_0) + Sel(I_1)$ when Sel=0 then the output data line connects to $I_0$ and for Sel=1 output connect to $I_1$.

For example, a generic unit of 2:1 mux may be used for 4:1 Mux, and a reduced three unit of 2:1 mux version can be used for the design of 4:1 Mux in a modular method. Fig. 3.2 (a) depicts the schematic and quantum depiction of a 4:1 multiplication in Fig 3.2 (b). The circuit layout for binary data is shown in Table 3.1, with select inputs represented by choose line inputs, based on the circuit architecture used for binary data.

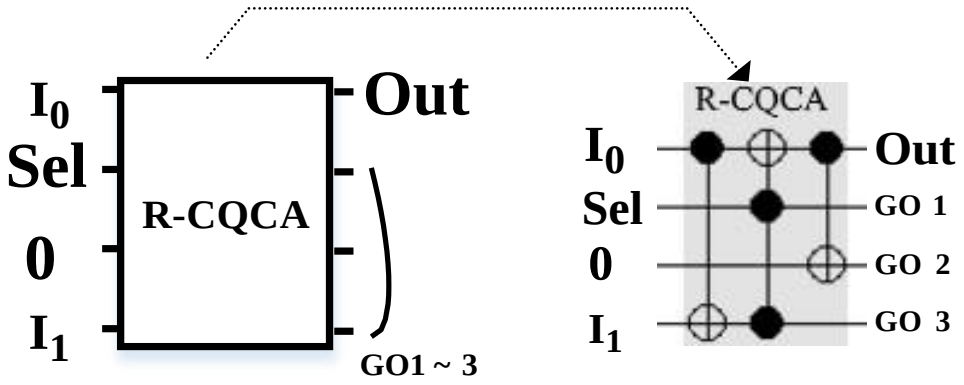
By combining two units of 4:1 Mux and one unit of 2:1 mux, we may create the 8:1 mux, whose construction is seen in Fig. 3.2. (c). A straightforward approach for multiplexer design is adopted in m: 1 mux design. Thus, the design of m: 1 mux has at least two units of $\frac{m}{2}$: 1 mux in addition to one unit of 2:1 mux. A complete construction for the execution of m:1 multiplexer is depicted in Fig. 3.2 (d). Thus, according to the modular approach of the multiplexer, lower bound reversible parametric analysis of the number of date inputs m is given by lemma 3.1. Algorithm 3.1 depicts a diagram of a building method for an m: 1 multiplexer. Table 3.2 depicts the computation process of data inputs in an 8:1 multiplexer circuit.

**Table 3.1 4:1** Data output form a multiplexer 4:1

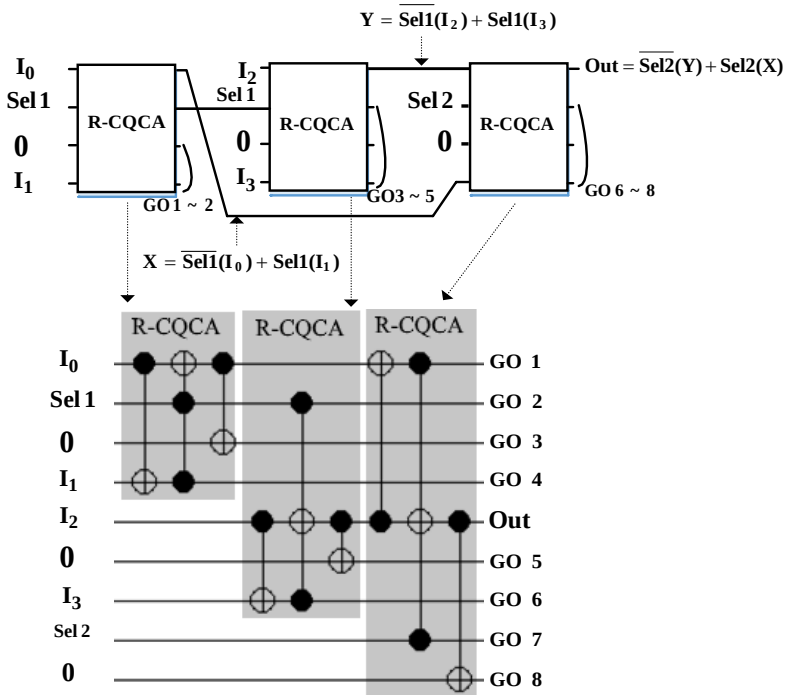
| $Sel_1$ | **$Sel_2$** | **X** | **Y** | **Out** |
|---|---|---|---|---|
| 0 | 0 | $I_0$ | $I_2$ | $I_2$ |
| 0 | 1 | $I_0$ | $I_2$ | $I_0$ |
| 1 | 0 | $I_1$ | $I_3$ | $I_3$ |
| 1 | 1 | $I_1$ | $I_3$ | $I_1$ |

**Table 3.2.** Data output from a multiplexer 8:1

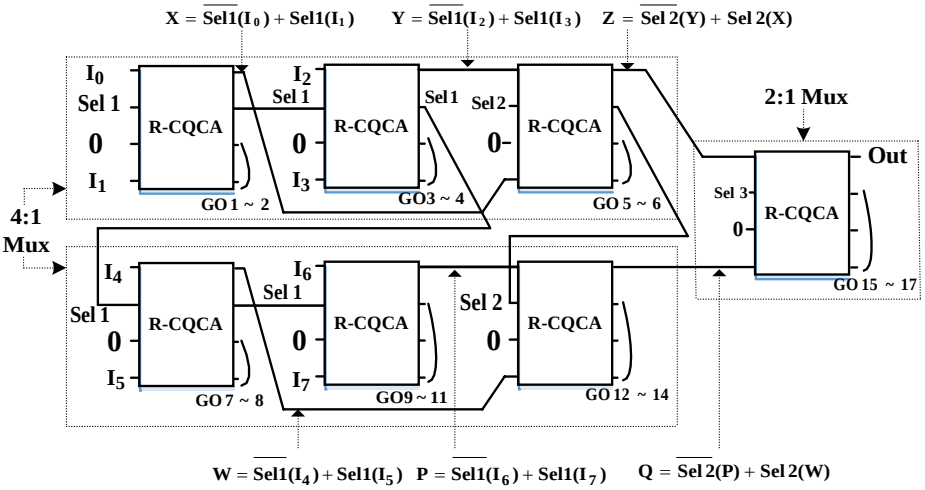
| $Sel_1$ | **$Sel_2$** | **$Sel_3$** | **X** | **Y** | **Z** | **W** | **P** | **Q** | **Out** |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | $I_0$ | $I_2$ | Y | $I_4$ | $I_6$ | P | $I_2$ |
| 0 | 0 | 1 | $I_0$ | $I_2$ | Y | $I_4$ | $I_6$ | P | $I_6$ |
| 0 | 1 | 0 | $I_0$ | $I_2$ | X | $I_4$ | $I_6$ | W | $I_0$ |
| 0 | 1 | 1 | $I_0$ | $I_2$ | X | $I_4$ | $I_6$ | W | $I_4$ |
| 1 | 0 | 0 | $I_1$ | $I_3$ | Y | $I_5$ | $I_7$ | P | $I_3$ |
| 1 | 0 | 1 | $I_1$ | $I_3$ | Y | $I_5$ | $I_7$ | P | $I_7$ |
| 1 | 1 | 0 | $I_1$ | $I_3$ | X | $I_5$ | $I_7$ | W | $I_1$ |
| 1 | 1 | 1 | $I_1$ | $I_3$ | X | $I_5$ | $I_7$ | W | $I_5$ |



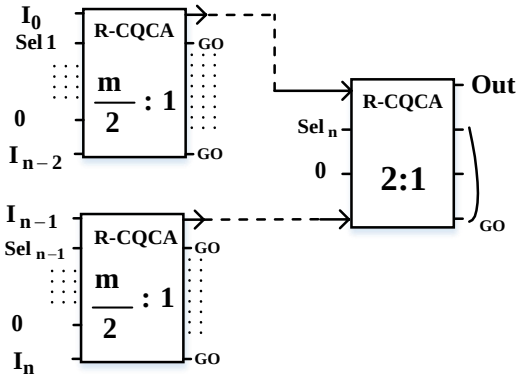

(a) Schematic diagram and equivalent quantum presentation of 2:1 mux using R-CQCA




(b) The schematic and quantum equivalent of 4:1 mux using R-CQCA




(c) Schematic diagram of 8:1 mux using R-CQCA




(d) The modular design of m:1 multiplexer

**Fig. 3.2** The proposed design of reversible multiplexer

**Lemma 3.1.** An m:1 multiplexer cascading link by the R-CQCA can be synthesized by (m-1) be the minimum gate count (GC) and constant input (CI), 2(m-1)+$\log_2 m$ be the garbage output (GO) and 4(m-1) quantum cost (QC)

**Proof.** The construction of m:1 multiplexer consists of $(\frac{m}{2}):1$ multiplexer and single 2:1 multiplexer. Hence the minimum GC and CI for 2:1, 4:1, 8:1 and m:1 type of multiplexer is presented in equations (3.1), (3.2) and (3.3).

$(GC)_{2:1\ mux}=(CI)_{2:1\ mux}$ =1= 2-1 (3.1)

Hence above equation hold for m=2.

$(GC)_{4:1\ mux}=(CI)_{2:1\ mux}$ =3 = 4-1 (3.2)

$(GC)_{8:1\ mux}=(CI)_{2:1\ mux}$ =7 = 8-1 (3.3)

Assume that the equations (3.1), (3.2) and (3.3) supports for m=n. Therefore an m:1 multiplexer can be synthesized by (m-1) gate count.

The GO rise by a 2:1, 4:1, 8:1 and m:1 type of multiplexer as drawn by equations (3.4), (3.5) and (3.6)

$(GO)_{2:1\ mux}$ = 3 = 2(2-1)+ $\log_2 2$ (3.4)

Hence above equation hold for m=2.

$(GO)_{4:1\ mux}$ = 8 = 2(4-1)+ $\log_2 4$ (3.5)

$(GO)_{8:1\ mux}$ = 17= 2(8-1)+ $\log_2 8$ (3.6)

As a mathematical induction, the least 2(m-1)+$\log_2 m$ garbage output for m:1 type of multiplexer.

A 2:1, 4:1, 8:1 type of multiplexer requires 4, 12 and 28 quantum cost. The quantum cost of m:1 multiplexer synthesize by induction as below equations (3.7), (3.8) and (3.9)

$(QC)_{2:1\ mux}$ = 4 = (2-1) x 4 (3.7)

Hence above equation hold for m=2.

$(QC)_{4:1\ mux}$ =12=(4-1) x 4 (3.8)

$(QC)_{8:1\ mux}$ =28=(8-1) x 4 (3.9)

Therefor a m:1 multiplexer hold the 4(m-1) relationship for QC.

**Algorithm 3.1** Modular-Design-Algorithm (m:1 multiplexer)

**Input, Output:** Input data set I=($I_0$, $I_1$, $I_2$,……,$I_{n-1}$), Select line Sel=($S_0$, $S_1$,……,$S_{n-1}$) and generate one output (Out) will store the outcomes.

**1.** **Begin**
Stage-1: Circuit takes 2 unit of $(\frac{m}{2}) : 1$ type multiplexer and 1 unit of 2:1 type multiplexer
**2.** **Begin procedure** (m:1 multiplexer)
**3.** **For** i=0 to m-1 **do**
**4.** **If** i=0 **then**
Utilize first $(\frac{m}{2}) : 1$ type multiplexer as an initial output of a $(\frac{m}{2}) : 1$ multiplexer
**5.** **End if**
**6.** **If** i=1 **then**
Utilize Second $(\frac{m}{2}) : 1$ type multiplexer as output of a $(\frac{m}{2}) : 1$ multiplexer
**7.** **End if**
**8.** **If** i=2 **then**
Choose the inputs of the 1 unit of 2:1 multiplexer from the cascade link from the 2 unit of $(\frac{m}{2}) : 1$ multiplexer
**9.** **End if**
**10.** **Else**
**Go to** line 2
**11.** **End for**
**12.** **Return** Select one desired output from 2:1 multiplexer, remaining output are consider as garbage output.
**13.** **End**

## The suggested conservative reversible multiplexer (R-CQCA) gate's layout designin QCA technology

The cell arrangement in QCA Designer is taken into consideration while evaluating the effectiveness of the proposed R-CQCA. Fig. 3.3, shows the R-CQCA cell layout in QCA technology. For result verification, the bistable-approximation engine is utilised in the QCADesigner tool. The findings are shown graphically in Fig. 3.4. The findings are represented by the fact that the polarisation values of diverse input combinations are very good value. Upon acquiring the simulation results in the QCADesigner tool the initial output P after a 0.25 clock cycle delay, the rest of the output P is obtained. After a one-clock-cycle delay, the third (R) and fourth (S) outputs are received. As a consequence of the application of cell layout and simulation to this proposed arrangement, which is shown in Lemma 3.2, three key properties (complexity, speed, and area) are obtained.

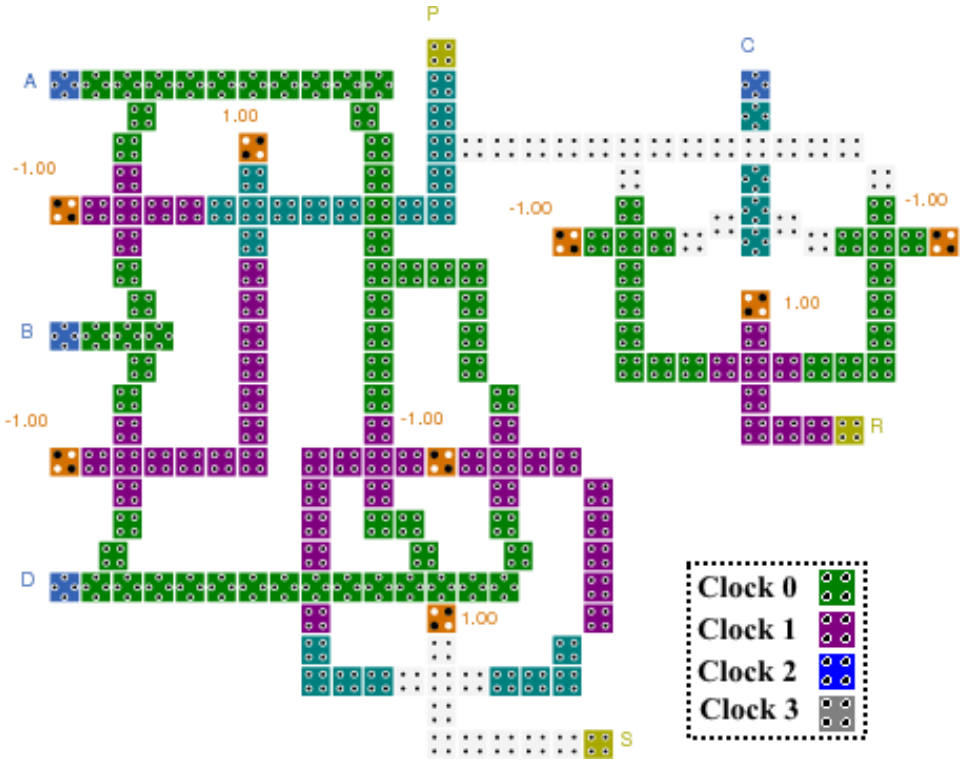



**Fig. 3.3.** Cell layout of R-CQCA

**Table 3.3** Comparative analysis results of Multiplexer design in QCA

| Design | Reversible | Cell calculations | MG | Inverter | Latency | Bounded-Area (μm$^2$) |
|---|---|---|---|---|---|---|
| **Chabi et.al. [37]** | No | 246 | 11 | 4 | 1.25 | 0.25 |
| **Teja et.al. [46]** | No | 124 | 9 | 9 | 2 | 0.25 |
| **Askari et.al. [47]** | No | 154 | 3 | 4 | 1 | 0.15 |
| **Sen et.al. [50]** | No | 23 | 3 | 1 | 1 | 0.02 |
| New | Yes | 177 | 9 | 1 | 0.25 | 0.24 |

**Lemma. 3.2** Using the results of simulations, the greatest delay needed to synthesise a 2:1 multiplexer is equal to 0.5

**Proof**. The cell arrangement in the 2:1 multiplexer is represented in Fig. 3.3. Cell layout in the 2:1 multiplexer Verification of the results is performed in QCA Designer using the bistable approximation model and the default settings. The simulation results demonstrate that when selecting input B= (0, 0), the outcomes P= (0, 1) arrive after 0.5 latency, i.e., when selecting input A= (0,1) and sending it to output node P is chosen and sent. When the inputs B= (1, 1) are used, the outcomes are P= (0, 1), which means that the input D= (0,1) is routed to the output node P. As shown in Fig. 3.4, the maximum latency of a 2:1 multiplexer is 0.5, which is consistent with the simulation results. As a result, the maximum delay of 0.5 is used for the 2:1 multiplexer.

**Table 3.3 compares multiplexers**

Table 3.3 summarises the reversible primitives and QCA primitives of multiplexer circuits mentioned before. Taking all reversible criteria into account, including gate count, garbage outputs, quantum cost, and conservative feature. All the parameters of the proposed multiplexer are presented in Table 3.4. Table 3.5 provides a full comparison of the existing and proposed multiplexer circuits. Recent previous work in Sen et.al [38], Malhotra et.al [48], Syamala et.al [49] contains certain reversible measures; the suggested modular method based multiplexer has the capacity of maximising all reversible metrics, which is not a significant advance. This is shown in Table 3.5, which depicts a comparative analysis table that shows that the suggested multiplexer circuits have sufficient evidence to be cost-effective.

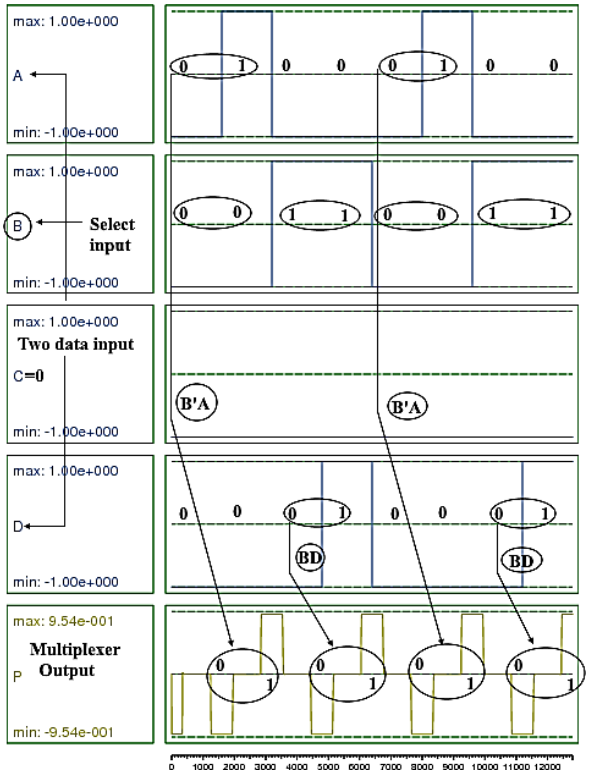



**Fig. 3.4** The outcome of a 2:1 multiplexer simulation using R-CQCA

**Table 3.4** Analyses of the suggested multiplexer's performance metrics

| Multiplexer | Metrics |
|---|---|
| **2:1** | 1 QC (R-CQCA) = 6 |
| | 1 GO (R-CQCA) = 4 |
| | 1 CI (R-CQCA) = 1 |
| | 1 UD (R-CQCA) = 1 |
| **4:1** | 3 QC (R-CQCA) = 3 x 6 = 18 |
| | 3 GO (R-CQCA) = 2 + 3 + 3 = 8 |
| | 3 CI (R-CQCA) = 1 + 1 + 1 = 3 |
| | 3 UD (R-CQCA) = 3 |
| **8:1** | 2 QC (4:1 mux) + 1 QC (R-CQCA) = 2 x 18 + 6 = 42 |
| | 2 GO (4:1 mux) + 1 GO (R-CQCA) = (6 + 8) + 3 = 17 |
| | 2 CI (4:1 mux) + 1 CI (R-CQCA) = 2 x 3 + 1 = 7 |
| | 2 UD (R-CQCA) = 2 x 3 + 1 = 7 |

Table 3.5 New multiplexer with the prior design of multiplexer

| Type | Parameters | Sen et.al [38] | Thapliyal et.al [39] | Malhotra et.al [48] | Syamala et.al [49] | Proposed |
|---|---|---|---|---|---|---|
| **2:1** | GC | 1 | 1 | 1 | 1 | 1 |
| | GO | 2 | 2 | 1 | 2 | 3 |
| | QC | 4 | 5 | 4 | 4 | 6 |
| | Conservative | No | Yes | No | No | Yes |
| | Equivalent quantum circuit | No | No | No | No | Yes |
| **4:1** | GC | 3 | 3 | 3 | 6 | 3 |
| | GO | 5 | 5 | 5 | 10 | 8 |
| | QC | 12 | 15 | 12 | 28 | 12 |
| | Conservative | No | Yes | No | No | Yes |
| | Equivalent quantum circuit | No | No | No | No | Yes |
| **m:1** | GC | (m-1) | 3n | - | - | (m-1) |
| | GO | (m-1)+$\log_2 m$ | 4m+1 | - | - | 2(m-1)+$\log_2 m$ |
| | QC | 4(m-1) | 15m | - | - | 4(m-1) |
| | Conservative | No | Yes | - | - | Yes |

'-' means- Not mentioned

## 3.4 CONCLUSIONS REMARKS

This proposed work is aimed at a new such as providing cost-effective solutions for confinement applications based on nano-electronics, which has been effectively shown in this chapter. The synthesiser circuits of conservative reversible multiplexer mentioned in this chapter are novel, and they have attained the desired results in their testing because of the parity preserving nature. The introduced reversible gate R-CQCA is optimal in circuits that are diametrically superior to one another. When compared to traditional multiplexer circuits, the modular method for multiplexer circuits offers superior performance metrics such as quantum cost and unit delay. The dependability of reversible metrics of the multiplexer is used by the use of lemmas. The inevitability of the ideal parameters for the m:1 mux is 2(m-1)+log 2m trash outcomes and 4(m-1) QC, which are the inevitable optimal parameters. The algorithm is useful for higher-order multiplexer design at the circuits, and its goal is to minimise the quantum cost and unit delay. The R-CQCA has a quantum cost of just six. Further investigation has been carried out to establish the influence of R-CQCA on QCA technologies. It is discovered that there is 2.5 latency and 195 cell complexity. The technology of QCA computing is used metrics such as complexity (cell count and gate delay), speed (latency), and the area would be made easier by using the suggested different kinds of a circuit (cell area and area usages).

# CHAPTER 4

# CONTENT ADDRESSABLE MEMORY (CAM) DESIGN USING QCA AND p-NML TECHNOLOGY

Content Addressable Memory (CAM) is a unique computer memory, which is used as cache memory and storage of data in very high-speed search computations within a single clock cycle. Unlike traditional Random Access Memory (RAM), CAM access data by searching its contents instead of searching the memory location of the content, Walas et.al. [63], Walas et.al. [64]. RAM is used only as a storage device and performs read or write operations, but CAM can store data, read or write data and also additionally compares data which makes it a good choice for applications that need the fastest speed searching, Cheng et.al. [65]. In many nano-scale computer processors and custom processors also CAM is used as associative memory as an extension to RAM as per Wang et.al. [66]. A CAM cell is a storage memory, where data can be directly accessed from the content itself instead of accessing memory or port addresses done by RAM (Random Access memory) in Walus et.al [63]. This is the main difference between CAM and RAM as data is directly accessed from the contents stored in the memory locations, it's widely used for search intensive applications. Concept wise CAM is similar to the data structure, logic of associative arrays, but the output of CAM is very simple logic making it preferable. So CAM is also called associate memory. There are three important basic operations performed by a CAM cell as Storage Operation, read and write operation and comparison or matching Operation as per Cheng et.al. [65]. In a storage operation like any other storage memory device, CAM also is used to store data. The data are automatically stored at a random location, no need to specify a memory location for storage. In reading and writing Operation, reads and searches have given input word from contents of stored memory, then searched word is specified which is made available to read, Writes given input word directly into memory storage accordingly. In comparison or matching operation the input data are searched against the contents of stored memory and compares the searched word and the input word for its matching to determine accuracy. Designing an energy-efficient CAM cell with less area and high-speed operations is complex and its various applications attract researchers in designing an efficient CAM.

The CAM cell, which is of single layer-based layout is introduced in QCA technology. The CAM cell is synthesised and implemented using the GDI-CMOS technique and QCA technology. The proposed design should be considered for achieving lower area, high speed and low power. The proposed CAM cells in both the GDI-CMOS design technique and QCA technology are to be compared by area, delay and power dissipation parameters to find out which technique of both is more efficient in the terms of low delay, low power and low area. The critical component in creating a CAM cell is to create an efficient circuit layout that utilises

sophisticated synchronous clocking schemes as the primary factor in synthesising any circuit architecture in the QCA technology.

Computing and memory elements are fundamental elements for all electronic devices. Presently CMOS technology is the backbone of these devices. However, there are some limitations for the further shrinking of this technology due to leakage current. Therefore, researchers are gathering towards alternative emerging technology. Among them, pNML technology is most promising due to the exciting features of nano-magnets in Robert et.al. [76]. The features are that there is no current flow, unlike CMOS technology. Here logic values are transferred from one magnet to another due to magnetic force, without physical current flow, this technology has ultra-low power consumption as per Fabrizio et.al. [77], Didem et.al. [78]. The second advantage of pNML is that it is non-volatile; therefore, it can store data for a long time. The third advantage is that it can design logic circuits in three dimensions (3D) which is saving the area. Therefore, its circuit density is improved compared to two-dimensional architectures.

## STATE-OF-THE-ART WORK FOR CAM MEMORY

This section discusses the previous circuit synthesis method.

### Prior Work of CAM Memory Using QCA Technology

The preferred design approach has been static CMOS technology for the past few years in Satyanarayana et.al. [55]. Attempts to propose better design approaches instead of static CMOS have been made to get better performance with limited area and power. Pass transistor logic (PTL) design came as one of the alternatives to static CMOS, which yields better performance with reduced area and power but the threshold drop significantly decreasing swing as per Zimmermann et.al. [69]. The design of VLSI digital circuit systems using GDI is known as GDI logic has been developed in the early 2000s, as per Satyanarayana et.al. [55]. The GDI technique is the best design method for digital circuits for reducing transistors with limiting power. Many new improved ways of designing GDI based circuits, CMOS hybrid circuits and the optimization of power and density with improved full swing was described in Foroutan et.al. [56]. One of the nano-technology approaches is QCA technology for designing digital systems is best suited for the high efficient computation and performance with less heat dissipation and less area in nano-scale integration of digital circuit designing, as per Vankammidi et.al. [51], Taskin et.al. [53]. Many new novel methods for clocking and efficient QCA gates was proposed in Ottavi et.al. [54]. The designing of the memory cell of one bit in QCA technology was done in line-wise based memory cell and loop wise based memory cell in Vankammidi et.al. [51]. The line-wise based memory cell has a major disadvantage as its design is complex and it needs more clock schemes or zones and increases the delay Frost et.al. [52], while the loop wise memory cell is easy to design and doesn't need more clock zones or schemes as feedback is used in this type of memory cell was studied in Taskin et.al. [53], Ottavi et.al. [54]. The QCA technology is used for designing CAM of one bit with easy circuit structure with the best performance and low power is introduced.

In light of that high-speed memory unit, match unit and the CAM cell architecture is introduced. Performance parameters show a higher level of performance in the introduced CAM memory is better than CMOS based CAM on high-speed computing applications. The CMOS based CAM cells are line-based memory cells. Different types of line based CAM cells

are designed using CMOS transistors and latches over the years for realizing a reduced power and area CAM cell which was discussed in Cheng et.al. [65]. Different CAM cells based online based memory are designed using the GDI design technique was presented in Satyanarayana et.al. [55]. The presented CAM cells have high performance with low power consumption. Memory cell designing in QCA technology prefers a loop-based memory scheme due to reduced clock cycles and area. Data is held in the memory inside the loop which was presented in Taskin et.al. [53], Berzon et.al. [60], Vankamamidi et.al.[51]. A conventional QCA RAM architecture based on loop and uses a 2 Dimensional grid of memory cells was described in Walus et.al. [63]. This proposed RAM has more storage ability. Addresses are accessed through grid lines of memory cells. An efficient and robust QCA based memory cell using a D flip-flop which is enabled using an edge-triggered clock was designed in Hashemi et.al. [71], which employed a set and reset ability. This proposed architecture does not use any crossover wires while designing memory cells as compared to previous memory cell designs. A robust RAM single layer cell layout using a five input majority gate in QCA technology was presented in Angizi et.al. [70], which has improved power consumption and area. The majority gate which is introduced is of low power, which is used as a building block in RAM cell. This designed RAM cell has better performance parameters compared to other memory cells. A new QCA CAM cell of a single layer layout was introduced in Heikalabad et.al. [72]. The CAM cell architecture introduces two parts memory and a match part. This CAM cell uses a unique five input minority gate for realizing the XNOR logic for match part was described in Angizi et.al. [70]. For memory, part realization is an RS flip flop based design was presented in Hashemi et.al. [71]. A unique low power inverter and a five input majority gate were introduced for designing a robust CAM single layer cell in Khosroshahy et.al. [67]. This presented CAM cell layout is simple with improved power and area parameters compared to Heikalabad et.al. [72]. The contribution should be present in the design of CAM cell layout because designing memory cells using QCA are less complex, also memory cells with high speed and low power.

The major contribution of this CAM memory towards QCA technology can be summarized as follows.

- Synthesis of the proposed memory unit, match unit and CAM cell in QCADesiginer tool and significant improvement in terms of majority gate, latency have been presented. There is no such attempt to the optimal value of primitives like cell count, majority gate, latency, and area of the circuit as compared with the literature.
- The energy dissipation aspect of the CAM cell layout is presented. To indicate the low power feature in this work. The extracted parameters of CAM cells are presented in Table and also compared to existing designs.
- Temperature versus polarization analysis of CAM layout based on the coherence engine in QCADesigner tool is presented.
- The proposed architecture of CAM memory using the GDI-CMOS technique has been presented. Further, the parameter analysis is done.
- QCA based simulations for the proposed CAM memory design are checked. Further, the area and delay are estimated.
- Compared both QCA technology and GDI-CMOS technique based proposed CAM cell and estimated the parameters like area, delay and power are evaluated. Efficient of above both technologies is concluded.

**Prior Work of CAM Memory Using p-NML Technology**

Several digital circuits such as Ex-OR gate, full adder, RAM memory is designed in three-dimensional pNML technology as per Cairo et.al. [79], Breitkreutz et.al. [80], Riente et.al. [81], Turvani et.al. [82], Riente et.al. [83], Garlando et.al. [84]. Here a new layout of CAM, which performance is superior to conventional Random Access Memory (RAM) is presented. The Content Addressable Memory layout in QCA technology is available in literature as per Heikalabad et.al. [85]. However, the demerit of QCA is that it is difficult to fabricate and for its operation, the cryogenic temperature is needed Sadoghifar et.al. [86]. So here, the CAM structure in pNML technology is introduced, which can operate at room temperature. For layout design, we have used the MagCAD tool, which is introduced in Riente et.al. [83].

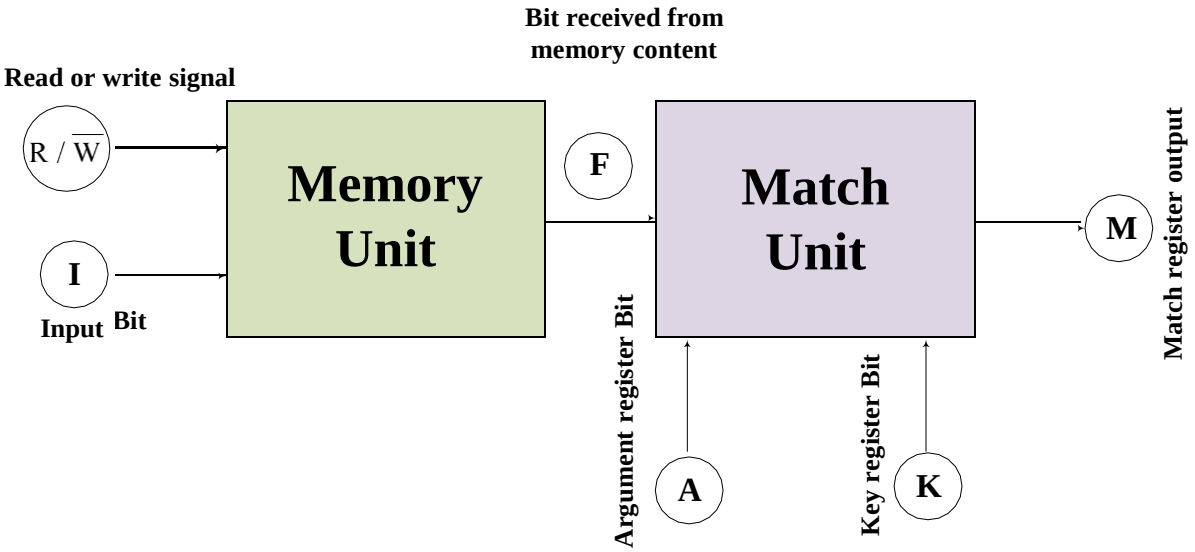
Synthesis of the layout of the memory unit and matching the logic design in pNML technology without changing the basic architecture of the memory unit and matching the logic gate have been presented. The growing need for small nano-electronics products is confining applications and associated applications to the synthesis of the design in developing technologies. The CAM memory architecture unit is the searching of data with high speed. Thus this synthesised layout is optimal based on parameters consideration such as total area, critical delay and latency. Thus, the designs presented are cost-effective based on parameters without changing CAM memory's fundamental structures utilising pNML technology. The pNML technique is used to fast the computing process, the performance of the design is analyzed by setting the magnetic width 220nm and grid size of 300nm, whereas iNML utilize 30nm magnetic width, 50nm magnet height, magnet H distance 10nm, Magnet V distance 10nm, number of clock phases 3, and clock zone max series 4. According to the above drawing setting, pNML utilize less magnet width and its 3D approach for design synthesizing. In this chapter, a pNML-based CAM memory is synthesised for the first time, according to state-of-the-art techniques. Area, critical delay and latency is a big impact on the circuit synthesis, therefore sometimes circuit designers compromise for layout consideration. However, in this suggested study, no parameters are sacrificed to the synthesis of CAM memory circuits. For introducing a cost-efficient CAM layout in pNML, the study shows optimal parameters such as area and latency. The proposed design of matching logic gates contains a 5-minority gate and 6- inverter and the memory unit consists of 3- minority gate and 4- inverter. The constructed architecture of CAM memory is optimized and can be used to miniaturization the area in designing complex architecture such as microcontroller and processor.

The proposed Content memory addressing architecture supports

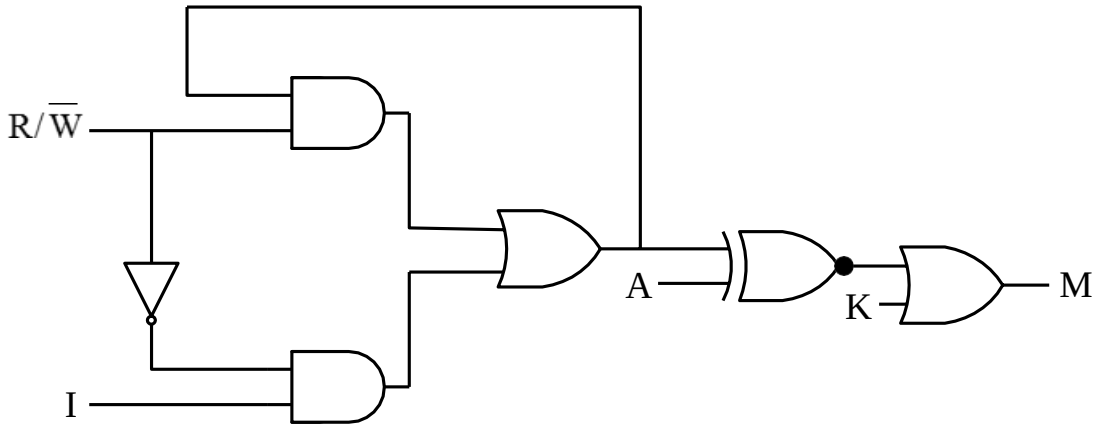
- A model of CAM memory is proposed by using pNML technology.
- The bounded box area of CAM memory 3.556 μm2 is evaluated.
- The cost-efficiency of the proposed CAM memory designs in pNML is investigated.
- The estimated latency at different input combinations for CAM memory is evaluated.
- Based on the minority voter gate a multilayer layout of CAM memory is synthesized with fast computation speed.
- The simulation results of CAM memory are verified and it's accurate like QCA and CMOS based design.
- Contrasting the novel CAM design with prior designs in consideration of parameters such as area and latency is investigated.
- The layout of CAM memory in pNML technology, which meets the requirement of nano-electronics confine application, based on performance parameters and physical existence has been investigated.

**The Proposed Work Related To CAM Memory Using QCA Technology**

CAM cell has two important operational units as memory unit and match unit. Two blocks such as memory and match operation is used to construct the CAM cell as depicted in Fig 4.1 (a). The logic diagram of the CAM cell consists of 2-AND, 2-OR, 1-XOR, and 1-NOT gates as depicted in Fig. 4.1 (b). To the memory block two inputs as R/W, and I are applied and one output F. Memory block output F is associated to match logic block as well as argument register bit (A) and key register bit (K). In the CAM cell design, two blocks such as memory and match logic are combined. Signal R/W signal is the input of the memory block. The acronyms are listed as K-Key register bit, A- Argument register bit, F- Bit received from memory contents, M- Match register output.




**(a)**




(b)

**Fig. 4.1.** CAM cell architecture (a) Block representation (b) Logic circuit

**Memory Unit**

The memory unit primary use is to perform read and write operations of the given input bit I as shown in Fig. 4.2 (a). The memory unit takes $R/\bar{W}$ and I as inputs and gives F as the output. Here $R/\bar{W}$ is read or write signal, I is the given input bit and F is the content bit received from the memory. The proposed CAM cell design is used on loop-based memory cell design. The $R/\bar{W}$ the signal is low, then the write operation is done by CAM cell. During a write operation, the given input bit I is stored in CAM at any random address in memory contents F and the same is taken at the output F. The memory cell design is a loop-based design instead of line based to reduce delay and components. If $R/\bar{W}$ is high, then read operation is performed. The bit to be read is searched in memory contents F and is marked to be read irrespective of given I input bit. The output F for a read operation is the same as the previous F memory content. A logical expression of CAM memory unit as $F = \{(R/\bar{W}).PrefF\} + (R/\bar{W}).I$

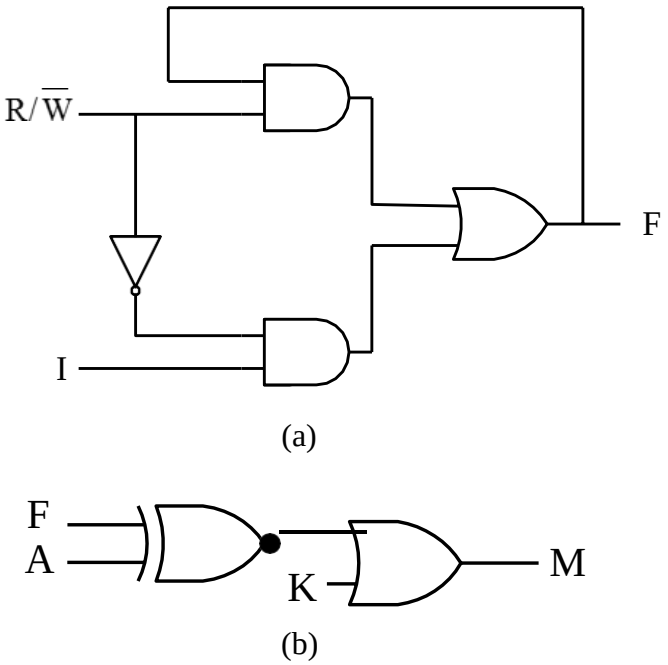



**Fig. 4.2** CAM cell modules (a) Memory operation unit of a single layer CAM cell logic circuit (b) Match unit of a single layer CAM cell logic circuit

**Table 4.1** CAM memory operation unit Truth table

| **Operation type** | **R/W Signal** | **I Input data** | **Pre F Value** | **F Output** |
|---|---|---|---|---|
| Write operation | 0 | 1 | X | **1** |
| Write operation | 0 | 0 | X | **0** |
| Read operation | 1 | X | 1 | **1** |
| Read operation | **1** | **X** | **0** | **1** |

Note: X-Don't care

### Match Unit

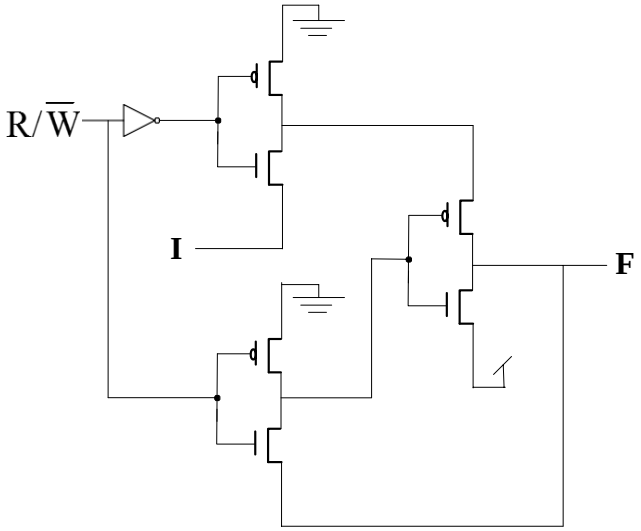
The match unit is primarily used for the searching and comparison operation of CAM cells in Fig. 4.2 (b). The output of the memory unit F is given as input to the match unit. Signals like F-bit received from memory content, A-argument bit and K- key resister bit is given as inputs to match unit and M- match bit is the output given by match unit. The M is always high when K is high irrespective of the $(\overline{A \oplus F})$ logic. But when K is low, M is high only when A and F are the same. In other cases, match register output M is low. Table 4.1 and Table 4.2 are truth tables of memory operation and match operation unit, respectively. The logical expression of CAM match unit as $M = (\overline{A \oplus F}) + K$

**Table 4.2** CAM memory operation unit truth table

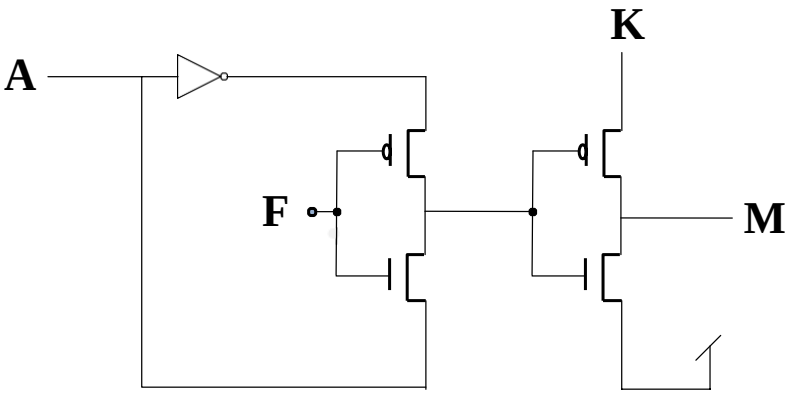
| **K**<br>**Key Register bit** | **A**<br>**Argument register bit** | **F**<br>**Bit received from memory contents** | **M**<br>**Match Register Output** |
|---|---|---|---|
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |

### GDI-CMOS Based Proposed CAM Cell

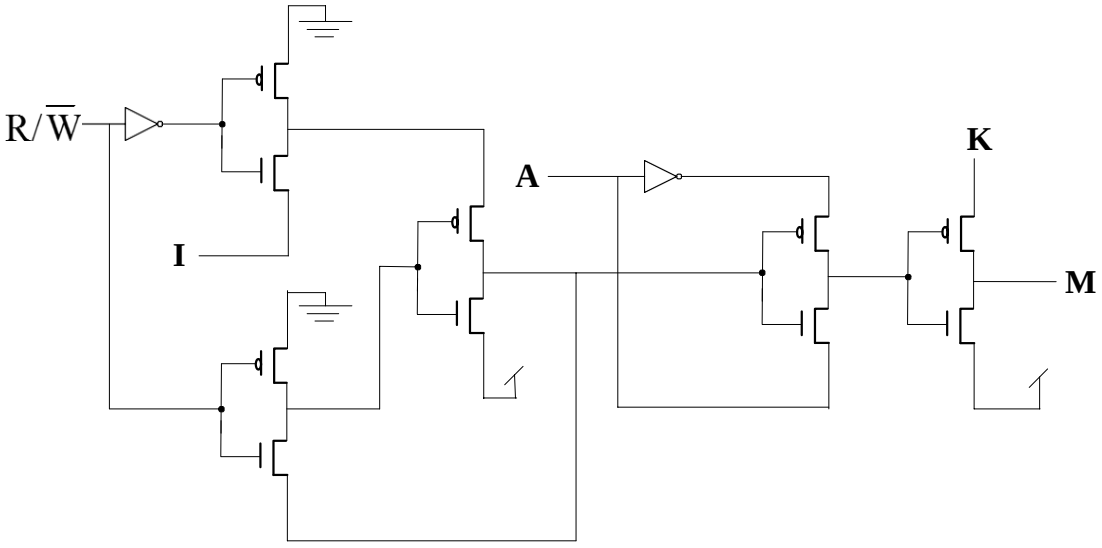
A GDI-CMOS based CAM cell structure is introduced, where memory is circulated inside a loop. The logic circuit of the proposed CAM cell memory CAM cell is designed in 35 nm process technology. The Figs. 4.3 (a), 4.3 (b) and 4.3 (c) show the schematic of the proposed blocks as memory operation unit, match operation unit and complete CAM cell, respectively. The simulation of designs in Figs. 4.3 (a), 4.3 (b) and 4.3 (c) verifies the functionality of proposed circuits like memory operation unit, match operation unit and CAM cell, respectively, which is drawn in Figs 4.4 (a), 4.4 (b) and 4.4 (c), respectively.




(a)

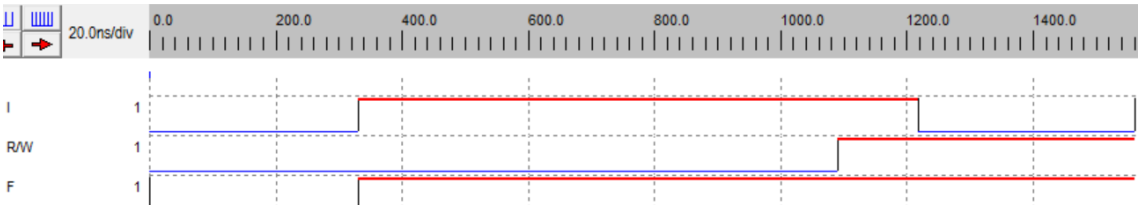



(b)

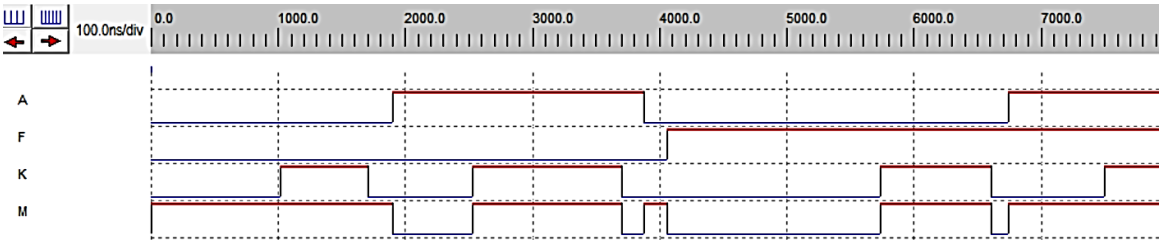



(c)

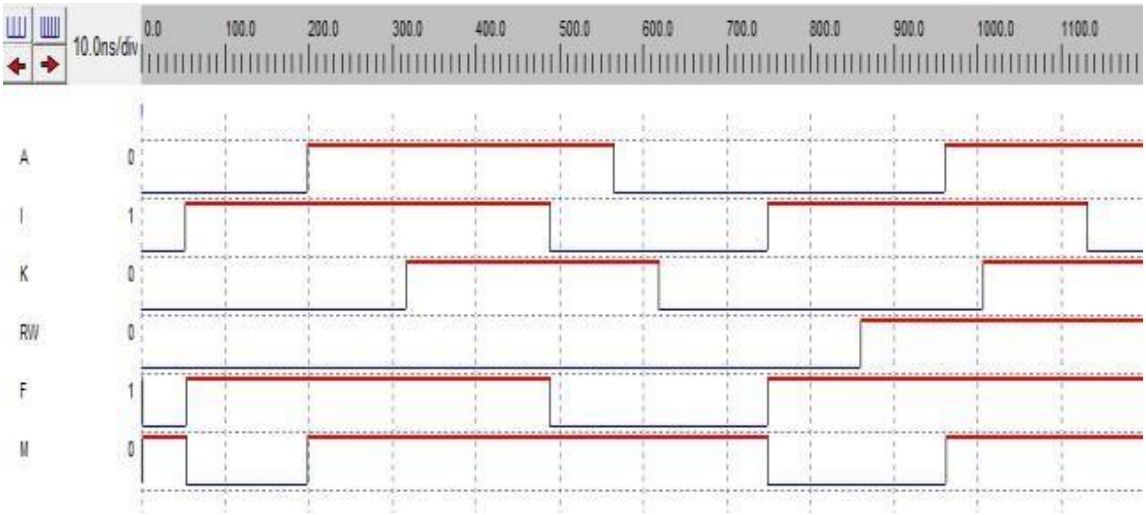
**Fig.4.3.** Design of proposed structures using the GDI- CMOS technique (a) Memory operation unit, (b) Match operation unit, (c) CAM cell




(a)




(b)

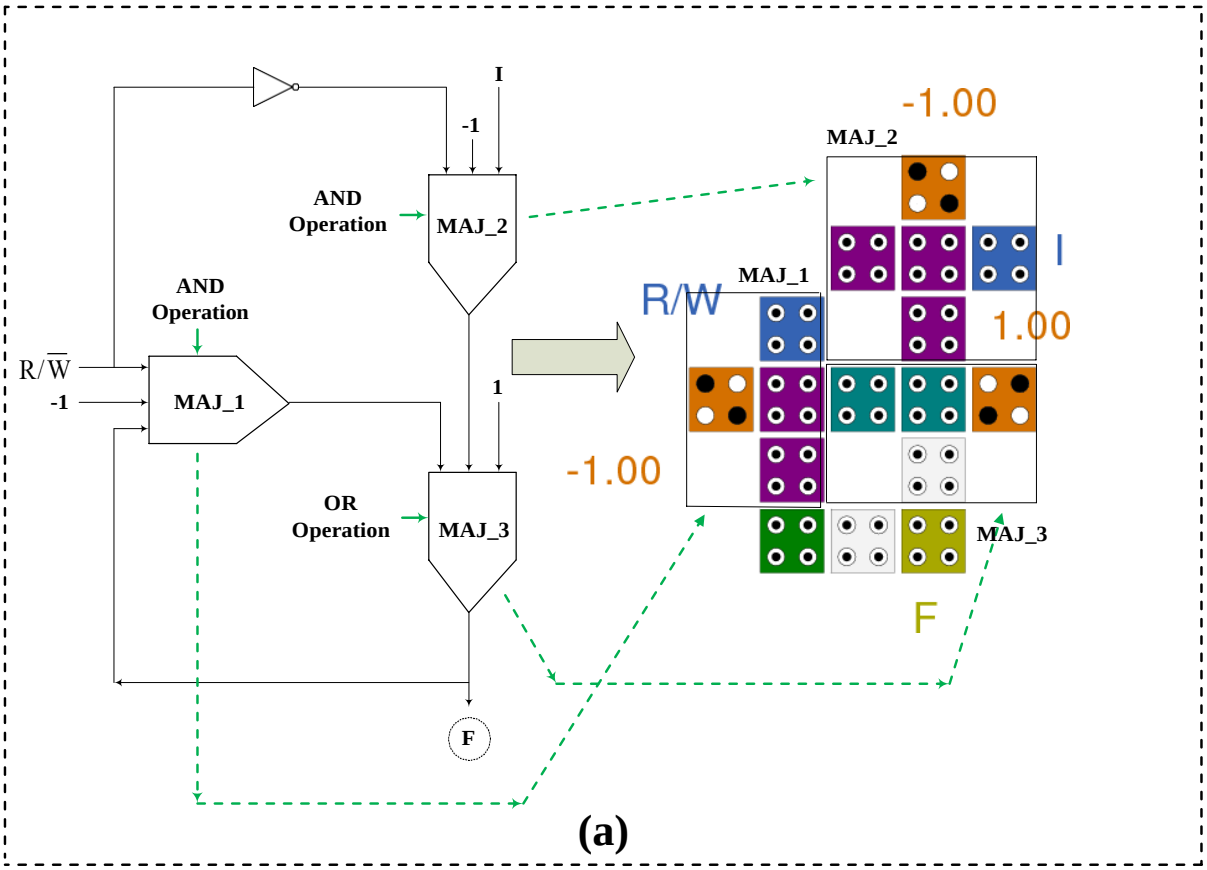



(c)

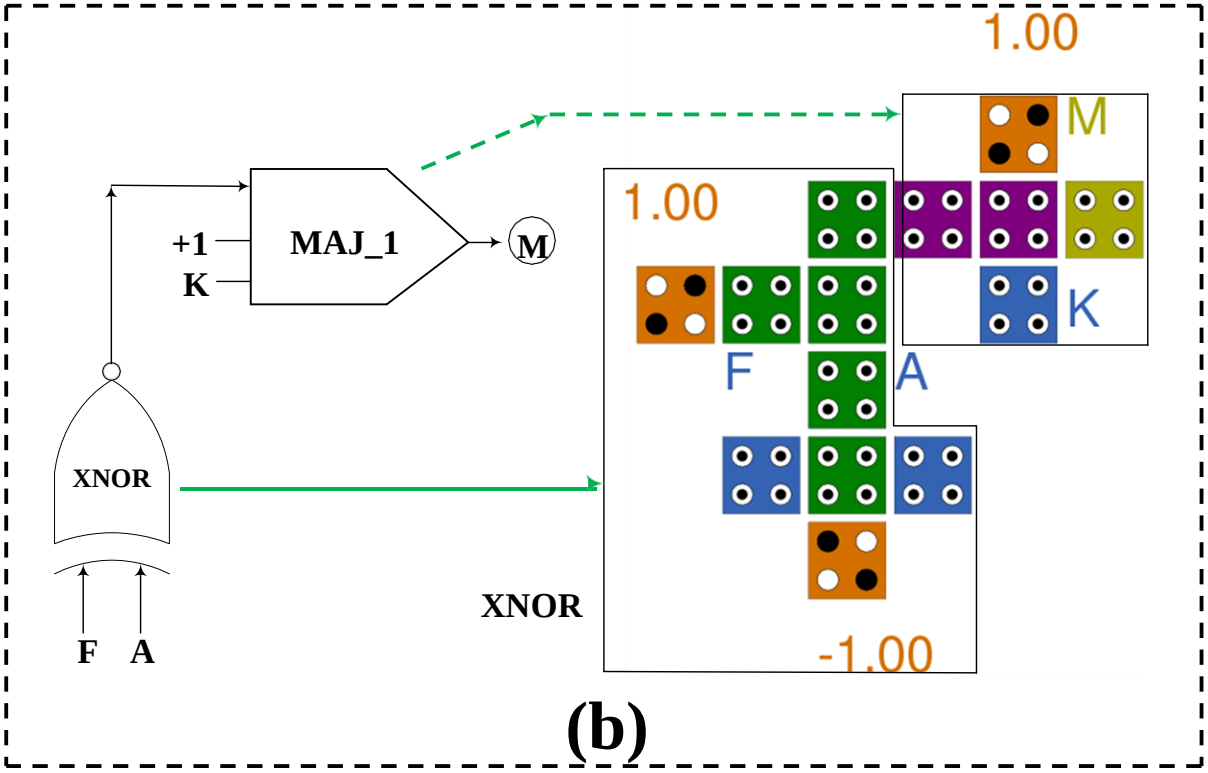
**Fig.4.4.** Simulations of proposed structures using the GDI-CMOS technique (a) Proposed Memory operation unit, (b) Proposed Match operation unit, (c) Proposed CAM cell

## QCA Based Proposed CAM Cell

The proposed structures of the memory operation unit, match operation unit, and CAM cell are designed, simulated and verified using QCADesigner 2.0.3 version software, Walas et.al. [64]. The simulation environment in the QCADesigner tool is set to follow default parameter values shown in Table 4.3. The size of the cell is 18 Sq. nm and dot diameter is 5 nm Wang et.al. [66]. The schematic and layout of proposed structures (memory operation unit, match operation unit and CAM cell) based on QCA technology is shown in Figs 4.5 (a), 4.5 (b), and 4.5 (c), respectively. The proposed structures like memory operation unit, match operation unit and CAM cell are simulated and the results are depicted in Figs. 4.6 (a), 4.6 (b) and 4.6 (c), respectively.


I
-1
AND
Operation
MAJ_2
AND
Operation
R/W̄
-1
MAJ_1
1
OR
Operation
MAJ_3
F
-1.00
MAJ_2
I
MAJ_1
R/W
1.00
-1.00
MAJ_3
F

(a)


1.00
M
+1
K
MAJ_1
M
1.00
K
F
A
XNOR
XNOR
F
A
-1.00

(b)

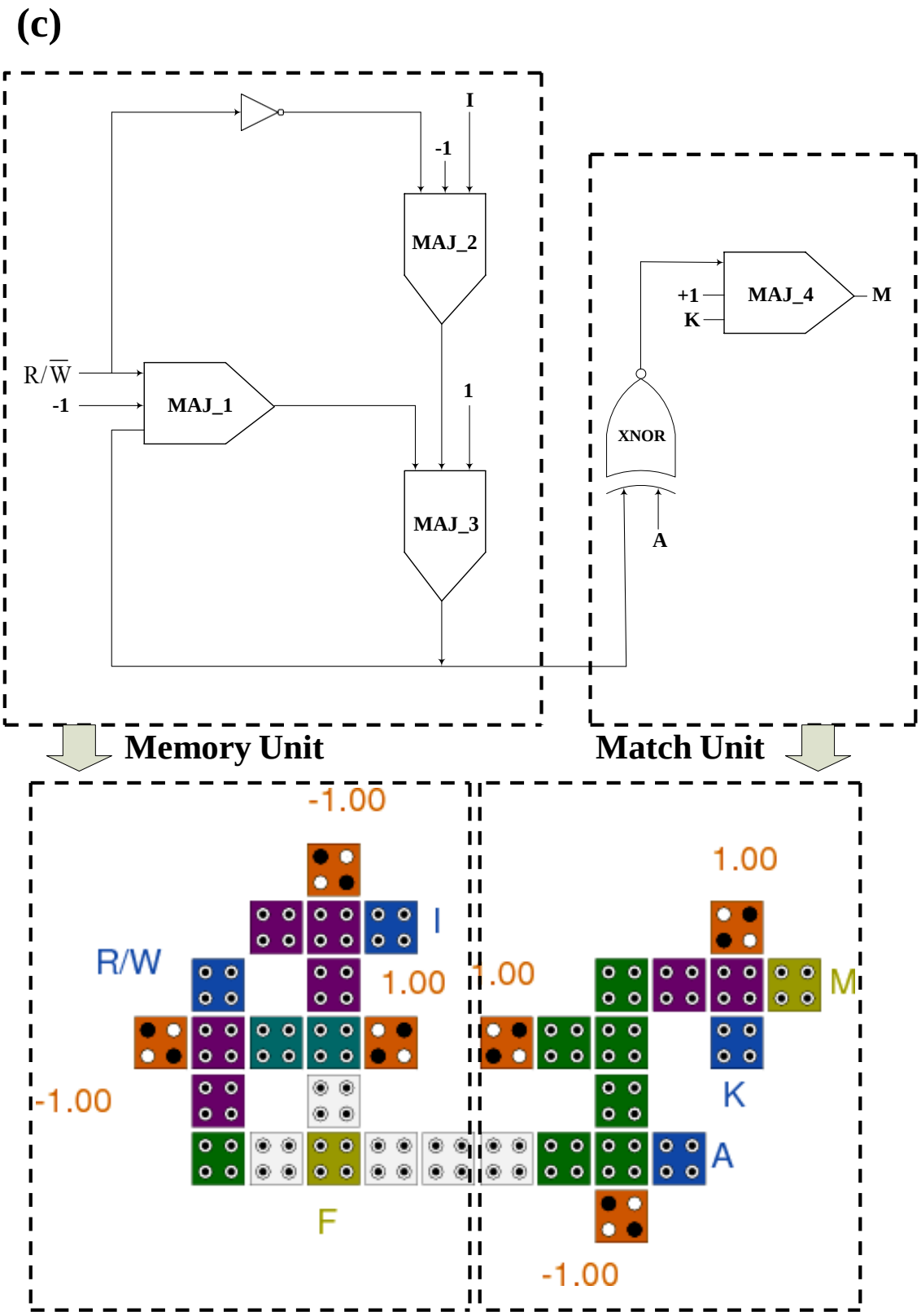
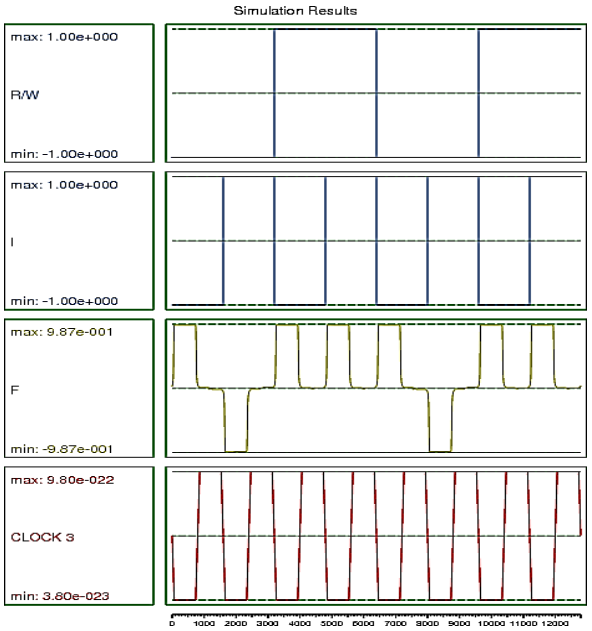
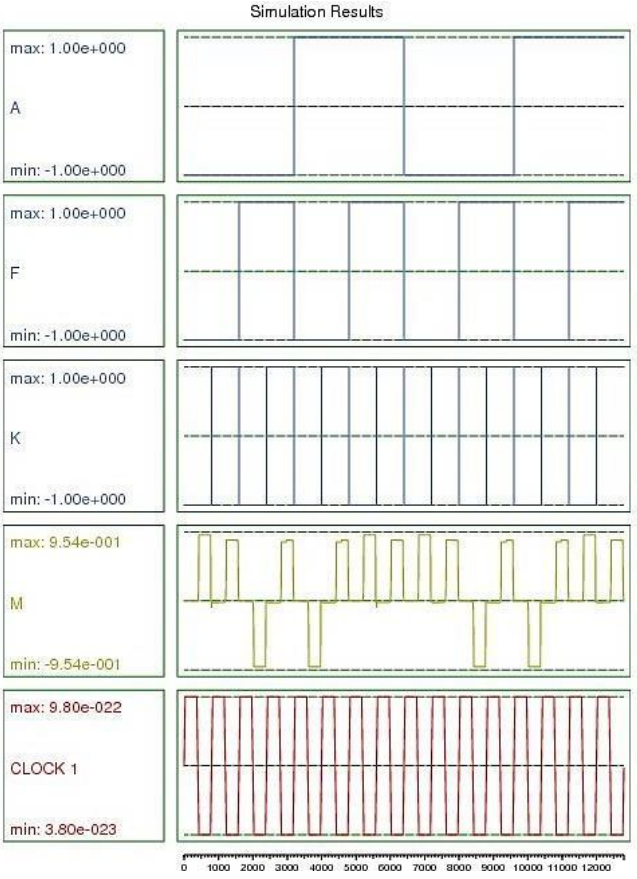


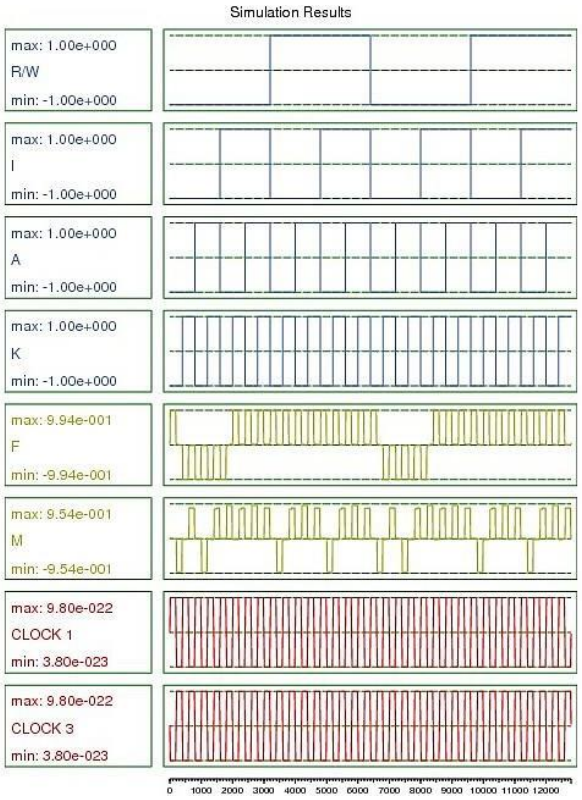

**Fig.4.5.** Design of proposed schematic and layout using a QCA technique (a) Memory operation unit, (b) Match operation unit, (c) CAM cell.


Simulation Results
max: 1.00e+000
R/W
min: -1.00e+000
max: 1.00e+000
I
min: -1.00e+000
max: 9.87e-001
F
min: -9.87e-001
max: 9.80e-022
CLOCK 3
min: 3.80e-023
0 1000 2000 3000 4000 5000 6000 7000 8000 9000 10000 11000 12000

(a)


Simulation Results
max: 1.00e+000
A
min: -1.00e+000
max: 1.00e+000
F
min: -1.00e+000
max: 1.00e+000
K
min: -1.00e+000
max: 9.54e-001
M
min: -9.54e-001
max: 9.80e-022
CLOCK 1
min: 3.80e-023
0 1000 2000 3000 4000 5000 6000 7000 8000 9000 10000 11000 12000

(b)




(c)

**Fig.4.6**. Simulations of proposed structures using a QCA technique (a) Memory operation unit (b) Match operation unit, (c) CAM cell

**Table 4.3** Default parameter values while simulating in QCADesigner software

| Layer Separation | High clock | Low clock | Clock shift | No. of samples | Convergence tolerance | Max.Iterations per sample |
|---|---|---|---|---|---|---|
| 11.5 | 9.80000 0e-022 | 3.8000 00e-023 | 0.000000 e+000 | 12800 | 0. 01 | 10 0 |

## Energy Dissipation Analysis of QCA Based CAM Memory

The QCA based proposed structure of CAM cell with energy analysis is done by using QCADesignerE software. The power dissipation of each cell can be analysed using QCADesignerE software as per Patidar et.al. [73]. The simulation conditions for energy analysis of coherence vector energy options which should be activated with energy are given in Table 4.4. The total energy dissipated along with the average energy dissipation per cycle of temperatures, 10K, 30K, 50K for the proposed structure is calculated in Table 4.5. Fig 4.7 gives an energy analysis, comparison of proposed CAM cell with prior presented CAM cell works in Khosroshahy et.al. [67], Heikalabad et.al. [72], performed at temperatures $1^0$K, $3^0$K, $5^0$K respectively. It can be determined from Fig. 4.7 that as temperature increases, the energy dissipation decreases because the polarization gradually slumps as temperature rises. The proposed CAM cell is more power-efficient compared to Khosroshahy et.al. [67] Heikalabad et.al. [72], by more than 50%.

**Table 4.4** Energy Analysis Simulation Conditions

| Options | On/Off |
|---|---|
| Euler Method | On |
| Runge Kutta | Off |
| Randomize Simulation Order | On |
| COS type clock signal | Off |
| RAMP type clock signal | Off |
| GUASS type clock signal | On |
| Zeroing of inputs | On |
| Display Energy Info of each cell | Off |
| Cell Coordinated(X/Y) | -1/-1 |

**Table 4.5** Power analysis comparison of Proposed CAM cell based on QCA technology with prior works

| CAM cells | Total-energy dissipation (eV) | | | Average- energy dissipation per | | |
|---|---|---|---|---|---|---|
| | $1^0$ K | $3^0$ K | $5^0$ K | $1^0$ K | $3^0$ K | $5^0$ K |
| Majority gate based CAM as per Khosroshahy et.al. [67] | 3.50e-002 | 3.35e-002 | 3.02e-002 | 3.18e-003 | 3.05e-003 | 2.74e-003 |
| Minority gate based CAM as per Heikalabad et.al. [72] | 3.38e-002 | 3.20e-002 | 2.55e-002 | 3.27e-003 | 2.91e-003 | 2.32e-003 |
| Proposed CAM | 1.98e-002 | 1.99e-002 | 1.91e-002 | 1.80e-003 | 1.81e-003 | 1.74e-003 |

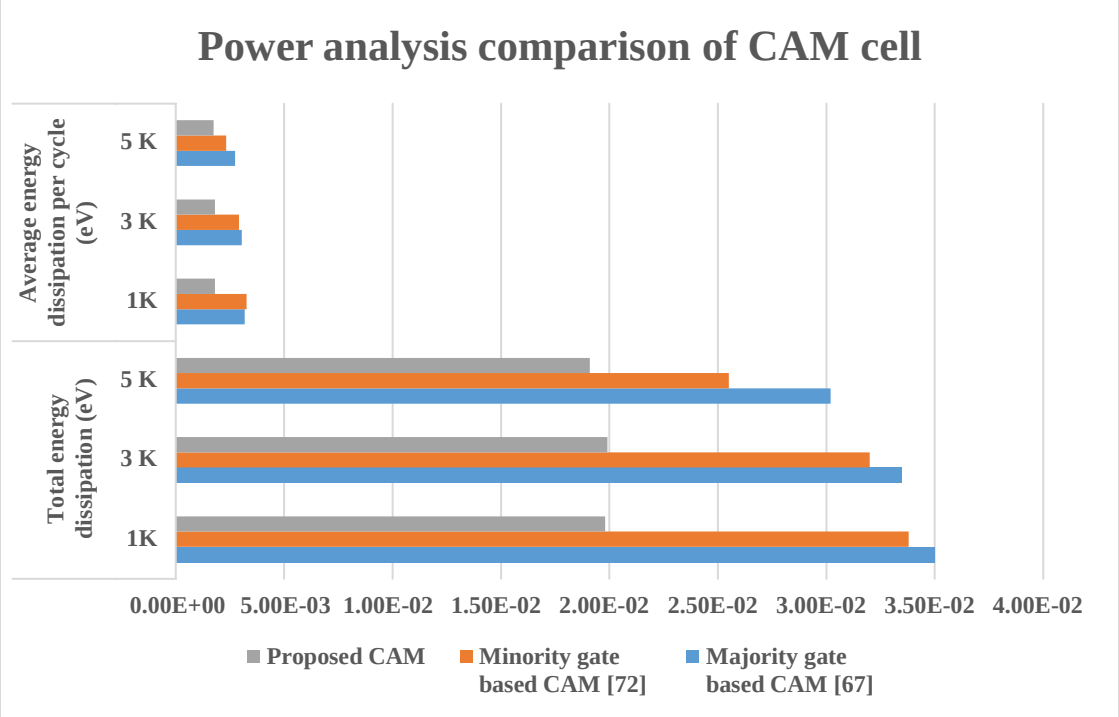



**Fig.4.7.** Graphical Representation of energy analysis, comparison of proposed CAM cell based on QCA technology with prior works as per Khosroshahy et.al. [67], Heikalabad et.al. [72]

### Temperature versus Polarization Analysis of The Proposed CAM Cell

The initial steady-state polarization across different values of temperatures are calculated and plotted in the graph shown in Fig 4.8. The stable performance of the structure is maintained at below $25^0$ K, here polarization is almost stable even with temperature fluctuations.

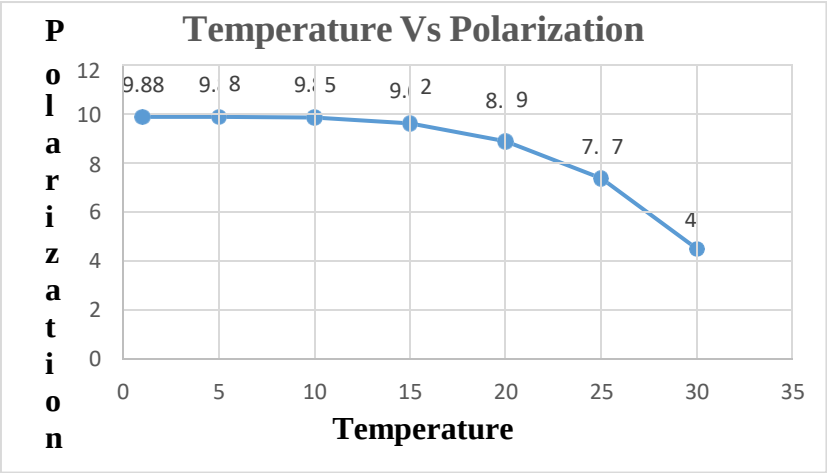



**Fig.4.8** Temperature deviation with Polarization graph for Proposed QCA-CAM

### The Performance Parameter Comparison between Proposed CAM Cell Using GDI-CMOS and QCA Technology

In this section, the performance parameter of the proposed CAM cell using GDI-CMOS and QCA is illustrated. Tables 4.6 and 4.7 gives the proposed structure parameter values for GDI based CMOS and QCA technology, respectively. Table 4.8 shows the proposed CAM cell based on QCA technology and CAM cell based on GDI-CMOS technique. The proposed GDI based CAM cell has an area of 2938.32 $\mu m^2$ and power dissipation of 367 mW. The proposed QCA based CAM cell has an area of 0.03$\mu m^2$ and power dissipation of 3.17 mW. The QCA based CAM cell has a low area, low power and fast speed performance compared to GDI-CMOS based CAM cell. The performance parameters of the CAM cell with the prior work is presented in Table 4.9.

**Table 4.6.** Parametric analysis of proposed structures using GDI-CMOS technology

| Parameter (units) | Proposed Memory Operation unit | Proposed Match Operation unit | Proposed CAM cell |
|---|---|---|---|
| Area in $\mu m^2$ | 1489.6 | 1031.6 | 2938.32 |
| Power dissipation (mW) | 0.144 | 0.171 | 367 |
| Number of transistors | 8 | 6 | 14 |

**Table 4.7** Parametric analysis of proposed structures using QCA technology

| Parameter(units) | Proposed Memory Operation unit | Proposed Match Operation unit | Proposed CAM cell |
|---|---|---|---|
| Area in $\mu m^2$ | 0.01 | 0.01 | 0.03 |
| Latency | 1 | 0 | 1 |
| Power dissipation in µW | 2.05 | 1.185 | 3.172 |
| Number of cells | 16 | 14 | 33 |
| Number of majority gates | 3 | 3 | 6 |

**Table 4.8** Performance comparison between proposed CAM cells based on GDI-CMOS and QCA technology

| Performance Parameters | Proposed CAM cell based on GDI-CMOS | Proposed CAM cell based on QCA |
|---|---|---|
| Area( $\mu m^2$ ) | 2938.32 | 0.03 |
| Power Dissipation (µW ) | 367 | 3.172 |
| Number of gates | 14 | 6 |

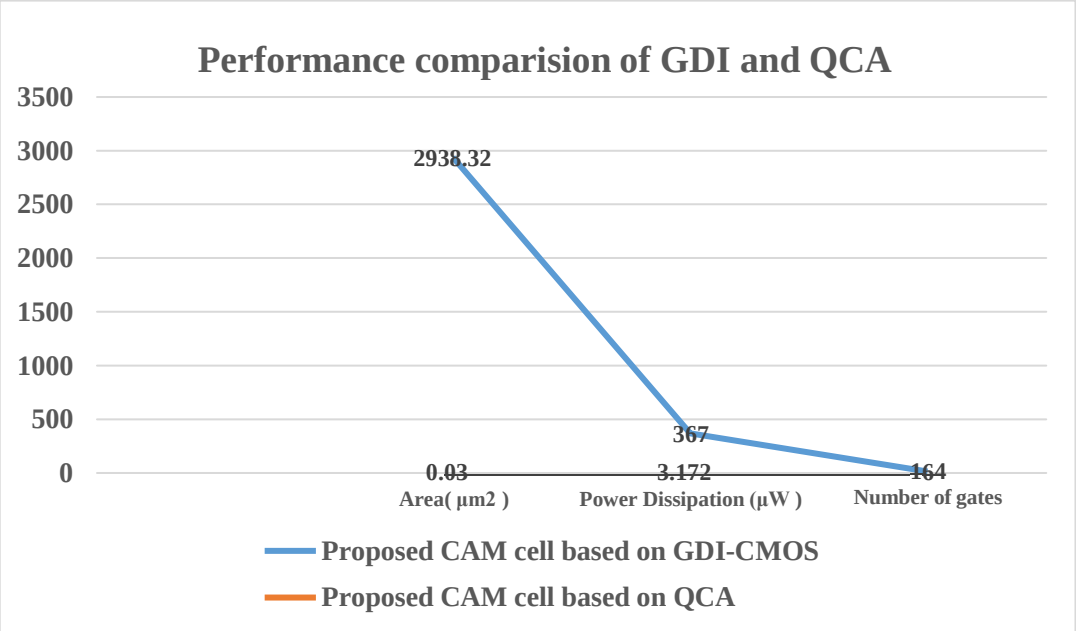



**Fig.4.9**. Graphical representation of Performance Comparison between Proposed CAM cell Based on GDI-CMOS and QCA technology

**Table 4.9.** Comparison of the newly memory and match cell with other published works

| Memory Cells | Total number of cells | Number of Majority gates | Latency (Number of clock cycles) | Area $\mu m^2$ |
|---|---|---|---|---|
| A Memory cell in Ref Sadoghifar et.al [74] | 23 | 3 | 1 | 0.03 |
| A memory cell in Ref Majeed as per [75] | 22 | 3 | 1 | 0.03 |
| New Memory | 16 | 3 | 1 | 0.01 |
| A Match cell in Ref Sadoghifar et.al [74] | 21 | 4 | 1 | 0.03 |
| A Match cell in Ref Majeed as per [75] | 15 | 3 | 0 | 0.02 |
| New Match cell | 14 | 3 | 0 | 0.01 |

**Table 4.10.** Performance Comparison of proposed CAM cell based on QCA technology compared to prior works

| **CAM Cell** | **Total number of cells** | **Number of Majority gates** | **Latency (Number of clock cycles)** | **Area $\mu m^2$** |
|---|---|---|---|---|
| RAM in Walus et.al. [63] | 158 | 8 | 2 | 0.16 |
| Majority gate based CAM in Khosroshahy et.al. [67] | 94 | 10 | 2 | 0.11 |
| Majority based RAM in Angizi et.al. [70] | 88 | 5 | 1.75 | 0.08 |
| Flip flop based RAM in Hashemi et.al. [71] | 109 | 8 | 1.75 | 0.13 |
| Minority gate based CAM in Heikalabad et.al, [72] | 100 | 10 | 2 | 0.14 |
| Sadoghifar et.al. [74] | 46 | 7 | 1.25 | 0.04 |
| Majeed et.al. [75] | 40 | 6 | 1.25 | 0.04 |
| New CAM cell | 33 | 6 | 1 | 0.03 |
| % improvement w.r.to Walus et.al. [63] | 79.91 | 25 | 50 | 81.25 |
| % improvement w.r.to Khosroshahy et.al. [67] | 64.89 | 40 | 50 | 72.72 |
| % improvement w.r.to Angizi et.al. [70] | 62.5 | NI | 42.85 | 50 |
| % improvement w.r.to Hashemi et.al. [71] | 66.97 | 50 | 42.85 | 62.50 |
| % improvement w.r.to Heikalabad et.al, [72] | 67 | 40 | 50 | 78.57 |
| % improvement w.r.to [24] | 28.26 | 14.28 | 20 | 25 |
| % improvement w.r.to [25] | 17.5 | NI | 20 | 25 |

NI-No improvement

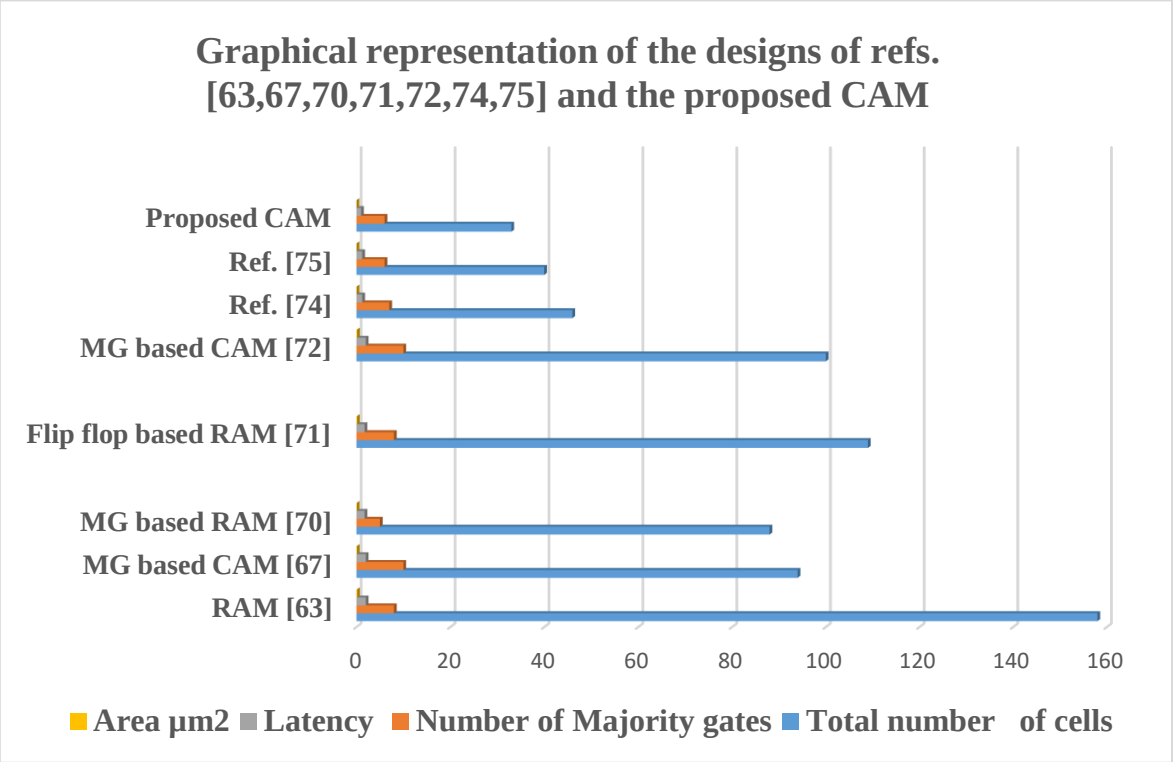



**Fig 4.10** Graphical representation of performance comparison between newly CAM cell based on GDI-CMOS and QCA Technology

The performance analysis of the memory and match with other published works is shown in Table 4.10. The comparison of GDI-CMOS and QCA is summarized in Fig 4.10. Compared to prior works as per Walus et.al. [63], Khosroshahy et.al. [67], Angizi et.al. [70], Hashemi et.al. [71], Heikalabad et.al. [72], Sadoghifar et.al. [74], Majeed et.al. [75] the proposed CAM cell is more improvements in the area, and delay is presented in Table 4.10. The proposed CAM cell as Table 4.10, more than 50% area improvement, less than 50% of QCA cells are reduced compared to prior CAM cell in Khosroshahy et.al. [67], Heikalabad et.al. [72]. The proposed CAM cell has a reduced number of cells and logic gates as calculated in Table 4.10. The proposed QCA based CAM cell is more performance, efficient in contrast to prior works presented in Khosroshahy et.al. [67], Heikalabad et.al. [72]. All the proposed work is dedicated to the GDI-CMOS and QCA technology. The proposed CAM cell, an improvement of 28.26%, 14.28%, and 20% and 25%, respectively, regarding cell count, number of majority gate, latency and area reported in Tables 4.10 as compared to the best existing design in Sadoghifar et.al. [74]. It can be seen that the proposed CAM cell design requires significantly less cell count compared with other best-reported designs in Sadoghifar et.al. [74], Majeed et.al. [75]. Also, the required area is less compared with other best designs in Sadoghifar et.al. [74], Majeed et.al. [75]. Consequently, this would lead to cost-efficient design. Moreover, the clock cycle delay of the CAM cell design is less than or equal to the other reported results which would result in a low delay in the circuit. The less propagation delay is desirable since it would allow high speed. The proposed CAM cell is implemented in the

QCADesiginer tool and has significant improvement in terms of majority gate, latency, reported in Table 4.10. There is no such attempt to the optimal value of primitives such as cell count, majority gate, latency, and area of a circuit such as a CAM cell in the literature.

## THE PROPOSED WORK RELATED TO CAM MEMORY USING pNML TECHNOLOGY

CAM is one type of storage device, which operation principle is searching for data with optimized speed. In this type of circuital memory, the time to obtain the searching item is very less. This working prototype of CAM is not the same as the RAM model since every memory area in CAM is required by its content. The proposed CAM circuit has two numbers of components, one of which is a memory unit and the other is a matching unit. For the matching unit, a new logic gate in pNML is proposed, which can improve the performance of CAM memory.

### The Proposed Matching Logic Gate

The pNML architecture of the logic gate that performs the matching operation and increases the CAM memory performance is shown here. The Boolean expression for this gate is $\text{out} = \bar{K}(A \odot F) + K$. This gate has 3 numbers of inputs i.e. A, K and F. Here F is the output of the memory unit that is fed to it and K input acts as a switch for the circuit. The principle of this gate is that if K= 0, then the comparison of the inputs A and F are done. Similarly, for K = 1, input values A and F are any value or named as don't care and output will be always 1. For example, if K = 0, A= 0 and F = 0, then in this case A and F values will be compared. Here both are the same, and then the output will be 1. If K = 0, A = 0 and F =1, then output will be 0. Table 4.11 is the truth table of the match operation unit. All the modelling equations 4.1, 4.2, 4.3. 4.4 and 4.5 are discussed below.

$$Y_1 = M1(A, 1, \bar{F}) = \bar{A}F \quad \textbf{(4.1)}$$

$$Y_2 = M2(F, 1, \bar{A}) = \bar{A}F \quad \textbf{(4.2)}$$

$$Y_3 = \overline{M(A,F)} = \overline{AF} = \bar{A} + \bar{F} + AF = A \odot F \quad \textbf{(4.3)}$$

$$Y_4 = \overline{M(K, Y_3)}$$

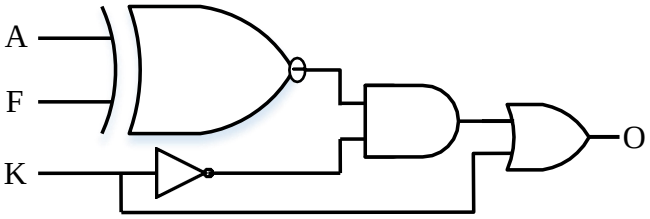
$$Y_4 = \overline{K + Y_3}$$

$$Y_4 = \bar{K}Y_3$$

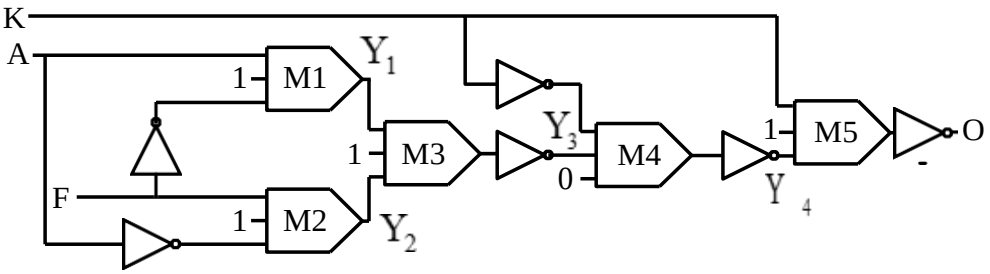
$$Y_4 = \bar{K}(A \odot F) \quad \textbf{(4.4)}$$

$$O = \overline{M(K, Y_4)} = \overline{K + Y_4} = \bar{K} + K$$

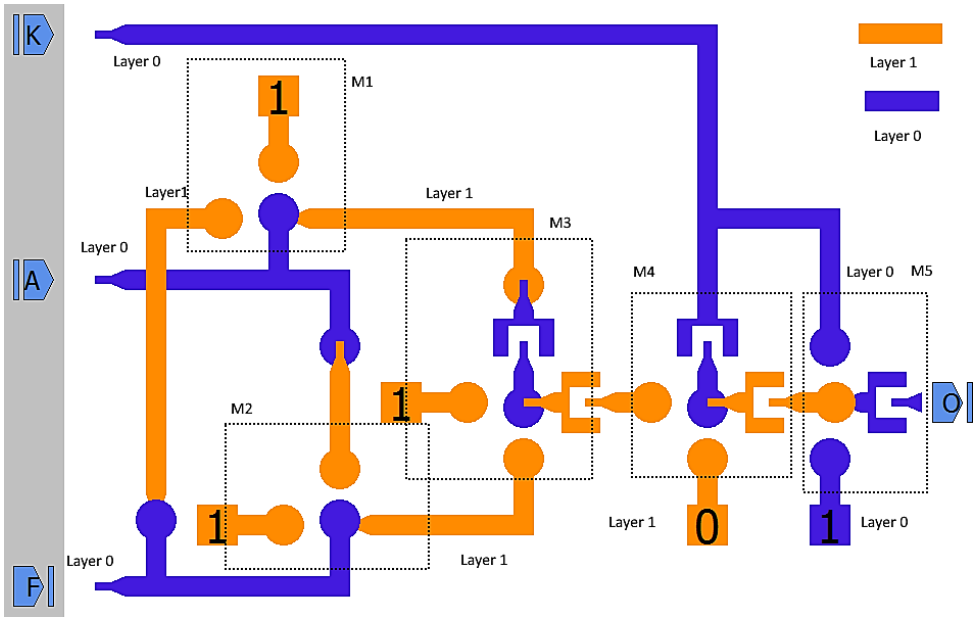
$$O = Y_4 + K = \bar{K}(A \odot F) + K \qquad (4.5)$$



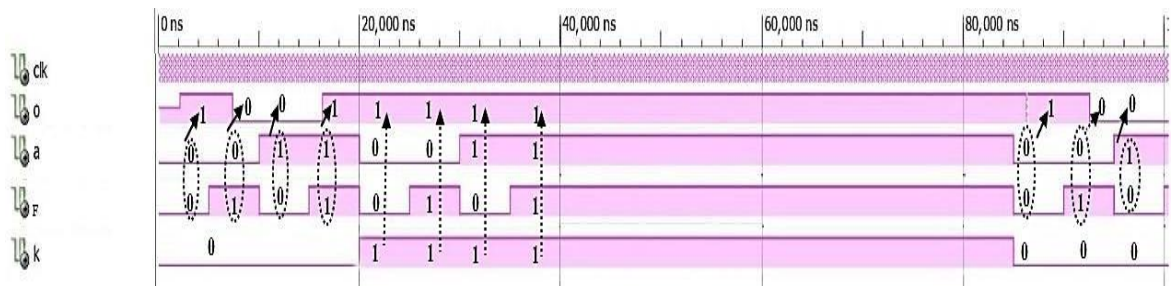

(a)




(b)




(c)




(d)

**Fig. 4.11**. Matching Logic gate (a) logic diagram (b) Minority vote based architecture (c) pNML structure (d) Simulation result

Fig. 4.11 (a) and Fig 4.11 (b), shows the logic gate and minority voter gate based Matching design. In Fig. 4.11 (c) the layout of the matching gate is shown. Its compilation result is illustrated in Fig. 4.11 (d). In this result, A, F, and K are the inputs, whereas O is the output.

**Table 4.11.** CAM match operation unit truth table

| K<br>Key Register bit | A<br>Argument register bit | B<br>Bit received from memory contents | O<br>Match Register Output |
|---|---|---|---|
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |

### 4.3.2 The Proposed Memory Unit

In the memory unit, there are two numbers of inputs i.e. R/W and I. When the R/W = '0', the input value of I will be reflected as output value F, as a consequence of the write input. By providing R/W ='1', the read operation is done. For example if operation= write, I = 1, R/W = 0 and previous F = any value, then output F = 1. If operation = write, I = 1, R/W = 0, previous F = any value, then output F = 0. If operation = read, I = any value, R/W = 1, then output F = 1. Similarly if operation = read, I = any value, R/W = 1, Previous F = 0, then output F = 1. Table 4.12 is the Truth table of the memory unit. The logic gate based design of a memory unit is shown in Fig. 4.12 (a). Fig 4.12 (b) shows the minority voter gate based architecture of the memory unit. The pNML layout of the memory unit is detailed in Fig. 4.12 (c) and its simulation result are shown in Fig. 4.12 (d). All the modelling equations 4.6, 4.7, 4.8, 4.9 and 4.10 related to the proposed memory unit design are presented below.

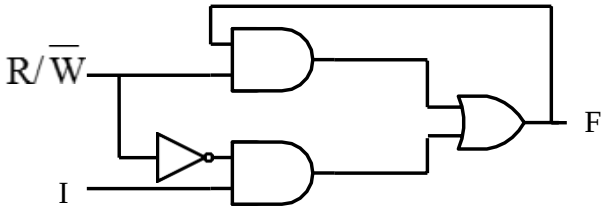
$$F = M3(M1(F, \overline{R/W}, 0), R, M2(R/W, I, 0)) \quad (4.6)$$

$$F = M3(F.\overline{R/W} + F + \overline{R/W}, R, R/W.I + \overline{R/W} + I) \quad (4.7)$$

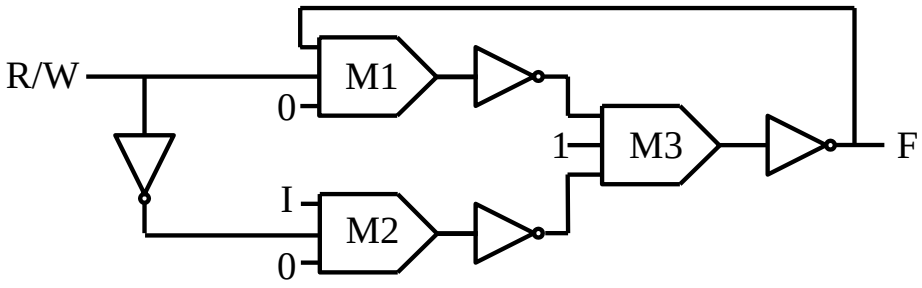
$$F = M3(F + R/W, R, R/W + I) \quad (4.8)$$

$$F = \overline{(\text{illegible})} \quad (4.9)$$

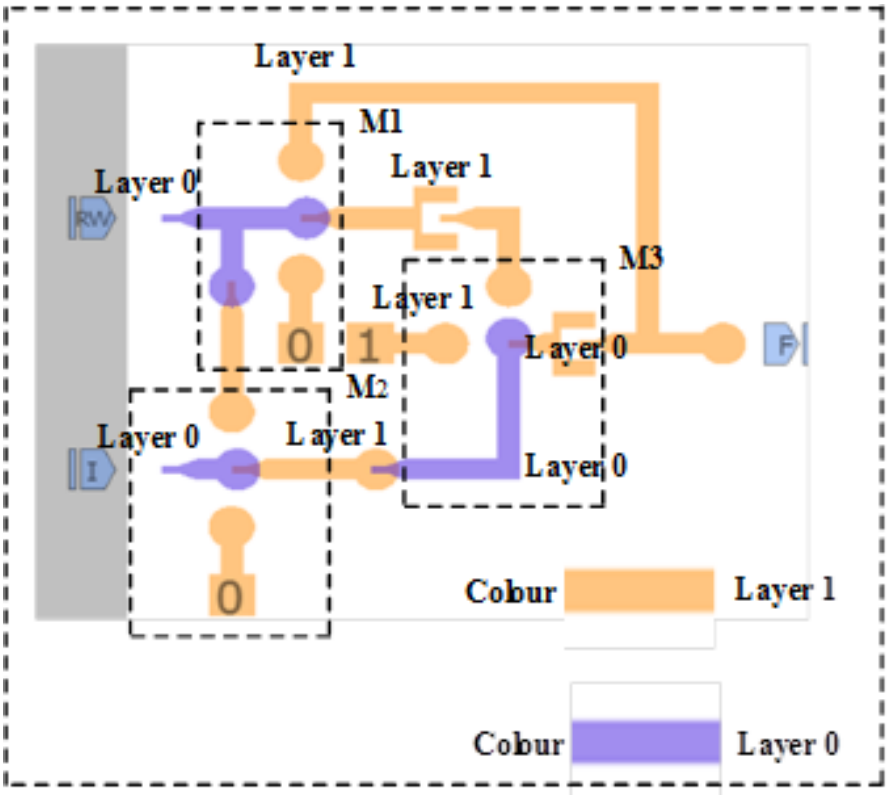
$$\mathbf{F} = (\mathbf{F}.\mathbf{R}/\mathbf{W}) + (\overline{\mathbf{R}/\mathbf{W}}.\mathbf{I}) \qquad (4.10)$$



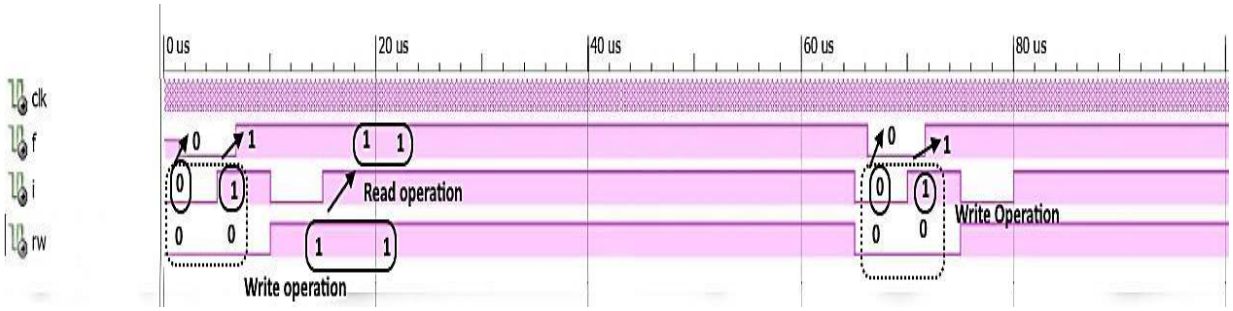

(a)




(b)




(c)




(d)

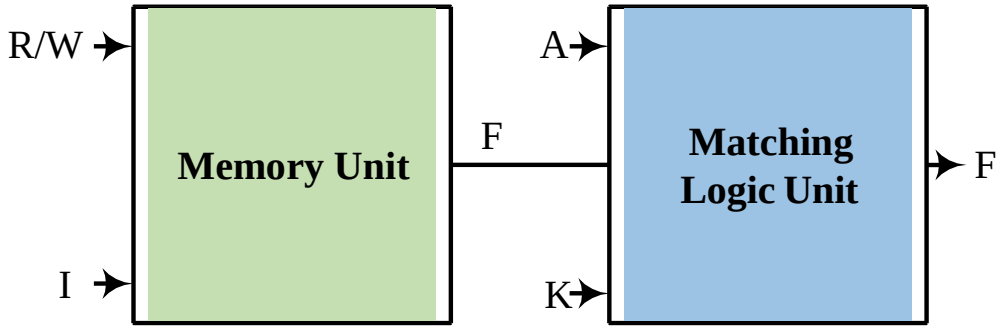
**Fig. 4.12** Memory unit design (a) logic diagram (b) Minority vote based architecture (c) pNML structure (d) Simulation result

**Table 4.12**. CAM-memory unit Truth table

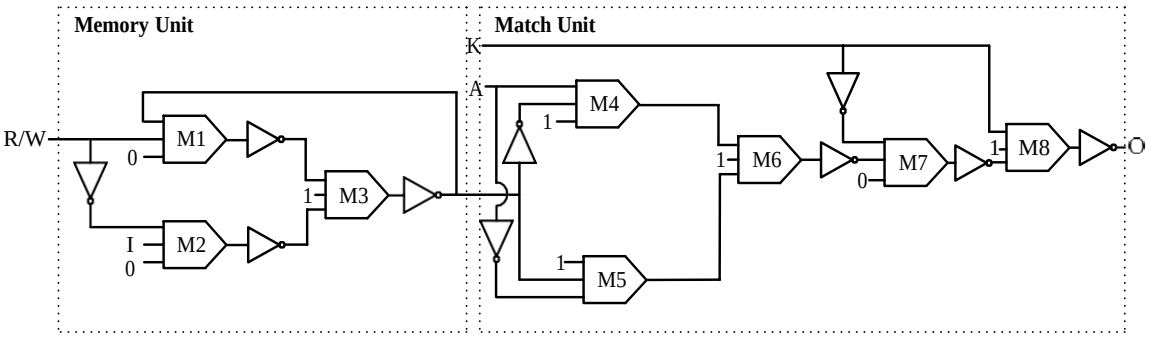
| R/W | I | Previous F | Output F | Remarks |
|---|---|---|---|---|
| **0** | 1 | X | 1 | Write operation |
| **0** | 0 | X | 0 | Write operation |
| **1** | X | 1 | 1 | Read operation |
| **1** | X | 0 | 0 | Read operation |

### 4.3.3. The proposed Content Address Memory (CAM) structure

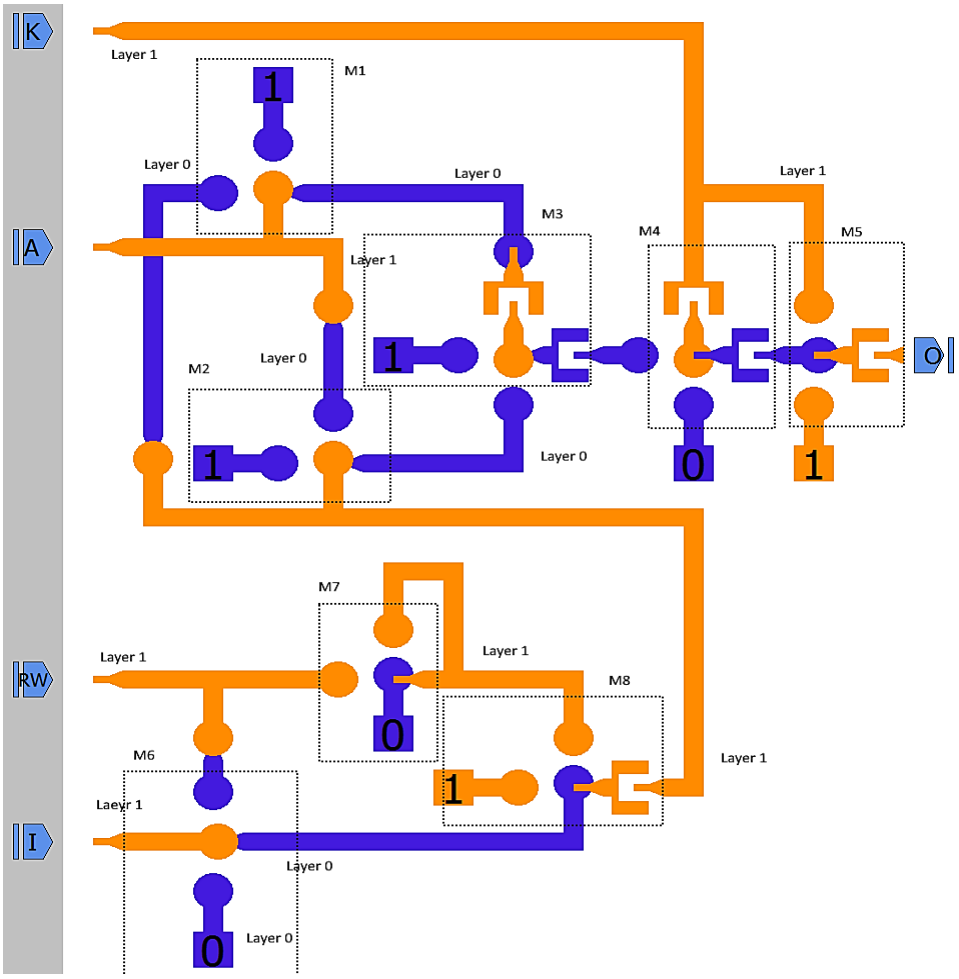
CAM is particular storage or memory type based on a lookup table. The one clock cycle here is adequate for the whole content of the data search. This allows us to seek the necessary data immediately and the memory gives a matching signal. Fig 4.13 (a) shows the block diagram of CAM design, this design utilizes two blocks one is a memory unit and the other one matching logic unit. The layout of Fig 4.13 (a) is presented in Fig 4.13 (c). The minority gate based design of CAM memory is presented in Fig. 4.13 (b). Fig 4.13 (c), presents the design of CAM memory in pNML, when grid size of 300nm and magnet width of 220nm. The performance parameters are also analyzed based on the synthesis tool MagCAD and it is observed the delay is lower as compared to QCA technology. Here the total circuit comprises a memory unit and a matching unit, which is designed by using the minority voter gate (Fig. 4.13 (b)). The output of the memory unit is given as an input to the matching unit. The pNML layout and simulation result is detailed in Fig. 4.13 (c). The right half of the pNML arrangement is the matching unit, with A and K as inputs, while the left half-section is the memory unit, with I and R/W as inputs. The memory unit's output is linked to the corresponding unit's input, and O is the final output as shown in Fig 4.13 (a).



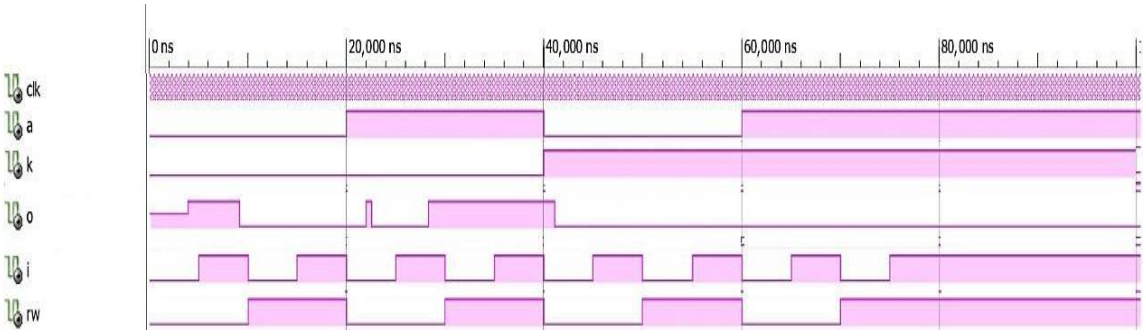

(a)




(b)




(c)




(d)

**Fig. 4.13.** The proposed CAM structure (a) logic diagram (b) Minority vote based architecture (c) pNML layout (d) Simulation result

The performance analysis is detailed in Table 4.13. In this table, five cases of input values are considered. If K = 0, there are four types of latency, the minimum latency is 3.91 E-6 second. If K = 1, the latency is 3.95 E-6 second.

**Table 4.13** Performance analysis of the Proposed CAM layout

| **3-D Content Addressable Memory Unit** | | | | | |
|---|---|---|---|---|---|
| **Total area= 3.556 μm$^2$** | | | | | |
| **Critical path delay= 1.679 E$^{-7}$ Sec** | | | | | |
| Inputs | | | | Output | Latency |
| K | RW | I | A | O | (in Sec) |
| 0 | 0 | 0 | 0 | 1 | 3.91 E$^{-6}$ |
| 0 | 0 | 1 | 0 | 0 | 4.16 E$^{-6}$ |
| 0 | 0 | 0 | 1 | 0 | 3.91 E$^{-6}$ |
| 0 | 0 | 1 | 1 | 1 | 3.91 E$^{-6}$ |
| 1 | X | X | X | 1 | 3.95 E$^{-6}$ |

## 4. 4 COMPARATIVE RESULT ANALYSIS

The suggested CAM memory is compared against many existing literature papers, as described in this part, to ensure that it is cost-effective. Table 4.14 shows a comparison of the newly developed CAM memory with certain existing literature articles. In comparison as per Sadoghifar et.al [86], Arsovski et.al [87], Lin et.al [88], Shafai et.al [89], Miyatake et.al [90], Lin et.al [91], Heikalabad et.al [92], Walus et.al [93], our design use optimal parameters in terms of delay. As evidenced from the comparison results presented in Table 4.15, the proposed designs yield better parameters such as area and latency as compared to other layouts in different technologies such as CMOS and QCA. The layout analysis of the novel CAM memory is verified by the MAGCAD tool.

The majority of research papers accessible in state-of-the-the-art work do not include a robust design, fast computing, and do not operate the device at room temperature. In terms of fast computing, area and operation at room temp, this propensity to apply current designs are inefficient. The suggested CAM memory architecture, however, improves latency. The area of the proposed design of CAM memory is optimized, and the other parameters of design are also studied and analyzed by setting the magnetic width of 220nm and grid size of 300nm in the MagCAD tool using pNML technology. The comparison results show the dominance of the novel CAM memory on the available reported designs in the literature. The proposed layout is cost-efficient, which can be considered as the base of architecture for planning complex processors. The pitfall of these conventional technologies methods such as QCA and CMOS is that they are utilized more delay. QCA devices are not operated at room temperature. Based on the literature review, the QCA device is difficult the device work at room temperature. The proposed CAM architecture that uses nonmagnetic logic, computes fast and practically can be possible at room temperature.

**Table. 4.14** The suggested CAM design is compared to current QCA and CMOS technology.

| Design technologies | Bounded Box Area | Clock cycle delay (Latency) | Technologies |
|---|---|---|---|
| Sadoghifar et.al. [86] | 0.14 $\mu m^2$ | - | QCA based |
| Arsovski et.al. [87] | 17.54 $\mu m^2$ | 3ns | CMOS Level |
| Lin et.al. [88] | 17.46 $\mu m^2$ | 2.7ns | CMOS Level |
| Shafai et.al. [89] | 232.2$mm^2$ | - | CMOS Level |
| Miyatake et.al. [90] | 1.73$mm^2$ | - | CMOS Level |
| Lin et.al. [91] | 0.53$mm^2$ | - | CMOS Level |
| Heikalabad et.al. [92] | 0.14 $\mu m^2$ | 2 | QCA based |
| Walus et.al. [93] | 0.16 $\mu m^2$ | 2 | QCA based |
| Hashemi et.al. [94] | 0.13 $\mu m^2$ | 1.75s | QCA based |
| Angizi,et.al. [95] | 0.08 $\mu m^2$ | 1.5s | QCA based |
| Heikalabad et.al. [96] | 0.14 $\mu m^2$ | 2s | QCA based |
| Majeed et.al. [97] | 0.11 $\mu m^2$ | 2s | QCA based |
| Khosroshahy et.al. [98] | 0.11 $\mu m^2$ | 2s | QCA based |
| Hashemi et.al. [99] | 0.13 $\mu m^2$ | 1.75s | QCA based |
| Angizi et.al. [100] | 0.08 $\mu m^2$ | 1.5s | QCA based |
| Walus et.al. [101] | 0.16 $\mu m^2$ | 2s | QCA based |
| Proposed | 3.556 $\mu m^2$ | 16.79 µs | pNML based |

## CONCLUSION REMARKS

The major contributions of this chapter are highlighted below:

- The proposed CAM cell of single-layer architecture in both GDI-CMOS based design technique and QCA technology is proposed and functionality is verified using simulations in both technologies. The performance parameters of the QCA technology-based CAM cell are far better than that of its GDI-CMOS based CAM cell counterpart. Furthermore, the proposed CAM cell in QCA technology when compared to other prior QCA memory cells has better performance with ultra-size density, low power, high-speed functions. The new designs such as memory, match and CAM cells show a great deal of efficiency for considering the primitives like the number of cells, delay and area allowing the synthesis of CAM parallel memory block. The proposed CAM cell can be further extended for more input bits and to build CAM parallel memory block.
- This work proposes a memory unit and match logic gate layout in pNML. The synthesized content-addressing memory in pNML is cost-effective, taking into account total area, critical path delay and latency. To make the CAM memory design more robust, with minimal latency and area, implementation of the proposed circuit is chosen with nano-magnetic technology with multilayer pNML method, which supports great benefit in synthesizing robust model of CAM memory. The total area used by the circuit is 3.556 $\mu m^2$ and the critical path delay is 16.79 µs. Therefore, this circuit is highly efficient in area and delay. The contribution of this article advances the CAM memory design by minimal parameters including total area, critical delay and latency to make the design cost-efficient. The proposed CAM architecture can be further extended for processor architectures in a three-dimensional domain.

# CHAPTER 5

# DIGITAL CIRCUITS USING 3D NANO-MAGNETIC LOGIC ARCHITECTURES

The size of devices is shrinking following Moore's law, with the result that every 18 months, twice as many transistors may be packed onto a single chip. However, beyond a certain degree of scaling, CMOS technology encounters some technical limitations, including limitations in terms of physical dimensions, power consumption, leakage current, higher lithography costs, and short-channel effects as per Stamp et.al. [102]. A new configuration of information processing is therefore being presented that is based on magnetism, in which interacting submicron magnets are employed to conduct logic operations and convey information at room temperature according to the researchers in Cowburn et.al. [103]. Nano-magnetic logic is the term used to describe this technique. It is not necessary to use transistors to execute magnetic operations at the nano-scale using this technology. Nano-magnetic components contain logical information in the magnetization direction and communicate this information to surrounding magnets via the dipole field coupling created by the magnetization direction. In addition to their scalability, nano-magnets have many other advantages such as their non-volatility (information is not lost while it is stored), their tolerance to radiation, the absence of leakage currents, and their very low power consumption Riente et.al. [104]. Consequently, the number of wires in the circuit is decreased, allowing it to overcome signal routing obstacles. At room temperature, it is possible to readily produce nano-magnets Pala et.al. [105]. Using nano-magnetic logic, it is possible to integrate memory and digital logic circuits into a single system composed of many layers of components. Per the direction of the magnetic field, nano-magnetic logic may be classified into two types: iNML and pNML, which are used when the magnetic field is in-plane or perpendicular to the plane, respectively. Many limitations of iNML are present, such as the restricted number of cascaded components, which necessitate the use of more than one clock pulse. Because of its inherent physical qualities, pNML technology is chosen, as is the fact that just a single clock pulse is needed for the system, making such circuits more compact and easier to build in Breitkreutz et.al. [106]. Domain wall conductors are used for signal routing in monolithic 3D circuits as per Becherer et.al. [107], Bhoi et.al. [108], Kimling et.al. [109], Breitkreutz et.al. [110], Ferrara et.al. [111], Turvani et.al. [112], Varga et.al. [113]. For the credibility of pNML computations to be assured, it was important to demonstrate time-dependent nucleation in field-based coupled nano-magnets Bhoi et.al. [108]. When employing perpendicular magnetic anisotropy in pNML technology, the domain nucleation field may be controlled, and it has been discovered that when the ends of a wire are built to have triangular points as opposed to a rectangular form, the switching field

can be reduced by 60% in Kimling et.al. [109]. Threshold logic gates may be realised using pNML technology, which is suitable for this purpose (TLGs). It was proved in Breitkreutz et.al. [110] that a TLG-based full adder (FA) architecture with five inputs based on a novel majority-vote (MV) gate could be implemented. In this state-of-the-art book, many digital circuits are detailed, including 4x 4 memory in Ferrara et.al. [111], one-bit FA designs Turvani et.al. [112], Varga et.al. [113], Garlando [114], combinational circuits such as comparators, decoders, and multiplexers in Misra et.al. [115], Misra et.al. [116], Pathak et.al. [117], and half-subtractors and code converters in Bhoi et.al. [118]. A durable, low-energy-dissipation approach was used in Erniyazov et.al. [119] to implement regular clock zones in QCA technology, which resulted in an appropriate solution for the adder design. In Riente et.al. [120], which is researching digital circuits based on nano-magnetic logic, a flexible EDA framework named ToPolinano is used to simulate and test numerous 3D digital circuits using a flexible EDA framework called ToPolinano. There have been developments in digital circuits based on QCA technology for combinational and sequential circuits, including even-parity generators Bahar et.al. [121] and multiplexers and demultiplexers circuits, as well as multiplexers and de-multiplexers Abdulla et.al. [122], Ahmad et.al. [123]. As a consequence of our literature study, we can provide novel parity generators, parity checkers, multiplexers, and ALUs for the first time, all of which are based on pNML technology.

The 3D pNML implementation of several digital circuits, including the Ex-OR gate, PG, PC circuits, 2-to-1 multiplexer, 4-to-1 multiplexer, and ALU capabilities, is discussed in detail in this chapter. pNML logic is used to synthesise the numerous digital circuits that are required. Based on the experimental results obtained with different kinds of magnets, it is evident that the newly proposed digital circuit architectures based on nano-magnetic logic accomplish better latency, area, and magnet count while incurring little hardware overhead. Finally, comprehensive simulations utilising the default settings for pNML technology are carried out to check that the new designs of the different digital circuits are functionally accurate. In the error detection and correction approach, PG and PC circuits are employed to identify and rectify errors. Multiplexing (mux) is critical in the selection of any one of the input signals from a large number of incoming input signals by utilising the data from the select line and forwarding it onto the output line, which is an important function. The arithmetic and logic operations performed by the ALU are utilised in the processing of data by the central processor unit (CPU). MagCAD, a bespoke layout editing programme, is used to create the circuit design. The MagCAD 2.10.0 utility is written in C++, but it is also accessible in a variety of other programming languages. The timing parameters, as well as a Verilog net list and technology description, are generated automatically by MagCAD after the design step is complete. MagCAD creates and exports the Verilog code for the circuit in a fully automated manner. Each component in the layout is interpreted differently in the extracted net list, which takes the shape of distinct items in the net-list form. Simulators such as Xilinx Vivado Design Suite may be used to generate simulation results, which can then be analysed. In addition, the calculating parameters, such as the bounding box area and latency, are discussed in more detail. In the synthesis of sophisticated control units for processor designs, the newly created digital circuits may be used as superior alternatives to the conventional ones.

The following are the primary pillars of the planned work:

- Compact architectures that include PG, PC, multiplexer, and ALU functions using pNML technology are demonstrated.
- Following the examination of the smallest limited area, the suggested design for the 2:1 multiplexer is equally valid for higher-order (4:1) multiplexer designs as it is for 2:1 multiplexers.
- The estimated latency of circuits with various types of functionality, such as PG, PC, multiplexer, and ALU, is examined for a variety of distinct input combinations.
- According to the custom layout design in pNML technology, the bounding box area of the suggested ALU is 58.59 $\mu m^2$, which is the maximum allowable area.
- It has been shown that simulation results obtained for the suggested designs with various functionalities such as PG, PC, multiplexer, and ALU functionality are comparable to those obtained from designs based on QCA and CMOS technology.
- The cost-effectiveness of the suggested designs is assessed by comparing them to the existing designs.

## THE PROPOSED DIGITAL CIRCUIT MODELS

This section describes the design of digital circuits based on nano-magnetic logic and pNML technologies, which are based on nano-magnetic logic. MagCAD 2.10.0 is used to create the custom layout of the suggested circuits such as the PG, PC, mux, and ALU. MagCAD 2.10.0 is a layout editing tool. Each circuit's functioning is checked to ensure that it is operating correctly following the required Boolean expression before it is used. To synthesise all of the layout designs in the custom layout editor, the pNML technology is implemented. All of the inputs to the custom layout are applied to utilise nucleation centres.

### The Newly Proposed Ex-OR Gate

An Ex-OR gate is a digital gate that performs an XOR operation on the digital inputs it receives. An Ex-OR gate gives a true (high or 1) output if the number of inputs with the value "1" is odd; otherwise, it produces a false (low or 0) output if the number of inputs with the value "1" is even. The output of a two-input Ex-OR gate will be "1" if both inputs are different, and "0" if both inputs are the same. The Ex-OR gate is seen schematically in Fig.

(a). Eq. 5.1 is a model for the mv gate-based Ex-OR. It is started as layer 0 type for the inputs (A and B). The input signals to mv1 are B, 1, and the inverse of A, while the inputs to the second are A, 1, and the inverse of B. According to Fig. 5.1 (b), the output of mv1 andmv2 is applied as an input to mv3, coupled with one fixed input of 1 and one variable inputof 0. The inverted output is always produced by the pNML layout. The Ex-OR arrangement,as shown in Fig. 5.1 (c), makes use of a total of three mv gates. A total area of 8.01 $\mu m^2$ has been allocated to the proposed model's bounding box. The simulation results for this 3D pNML configuration of the Ex-OR gate are shown in Fig. 5.2. As shown in Table 5.1, the calculation table for four distinct combinations of parameters, as well as the latency findings,

have been assessed and summarised.

Where $C = \overline{M_3\left(1, M_1\left(1, \overline{A}, B\right), M_2\left(1, A, \overline{B}\right)\right.}$ (5.1)

$$= \overline{M_3\left(1, \overline{\overline{A} + B}, \overline{A + \overline{B}}\right)}$$

$$= \overline{M\left(1, A\bar{B}, \bar{A}B\right)}$$

$$= \overline{\overline{A\bar{B}} + \overline{\bar{A}B}} == \overline{A\bar{B}} + \overline{\bar{A}B} == AB + \bar{A}\bar{B}$$

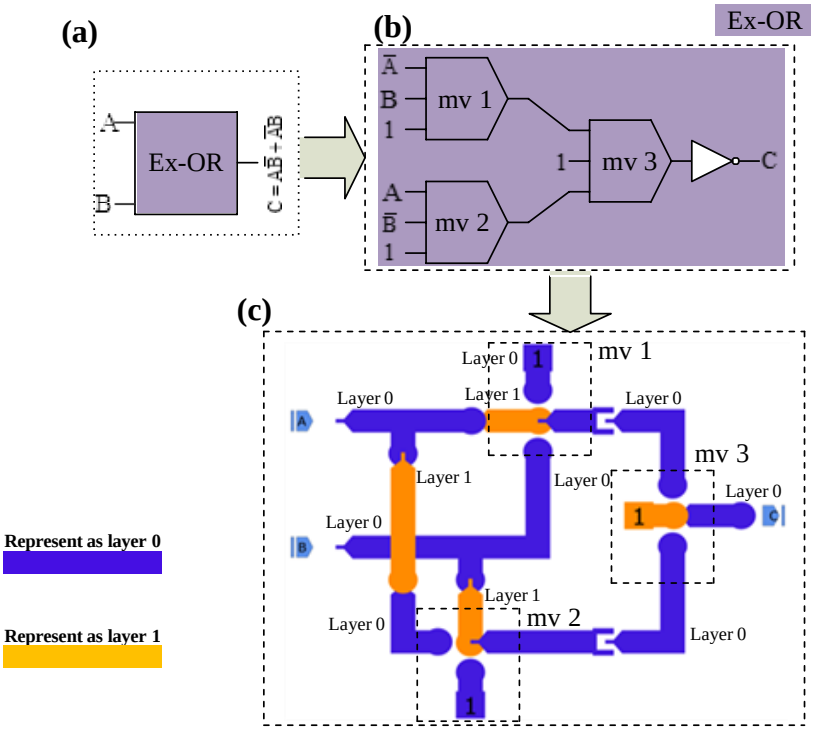



**Fig. 5.1.** The proposed Ex-OR gate (a) Schematic (b) pNML block diagram (c) pNML architecture

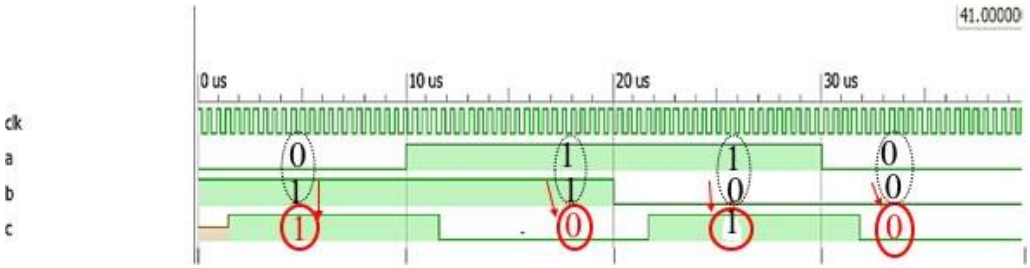



**Fig. 5.2** Simulation result of the Ex - OR gate using nano-magnetic logic-based pNML

**Table 5.1** Computational Table of Ex-OR gate

| Inputs | | Output | Latency(in sec) |
|---|---|---|---|
| A | B | Y | |
| 0 | 0 | 0 | $1.79E^{-6}$ |
| 0 | 1 | 1 | $1.41E^{-6}$ |
| 1 | 0 | 1 | $1.75E^{-6}$ |
| 1 | 1 | 1 | $1.81E^{-6}$ |

## The p-NML Technology-based Even-Parity Generator Circuit

The PG circuit is a sort of combinational circuit that is used to create the parity bit, which is a common approach for detecting data transmission problems during transmission. It is necessary to include the parity bit in the sent data stream to maintain error control. In

the case of an even-parity generator, the addition of a parity bit of "0" to the data stream shows that there are an equal number of "1" values in the transmitted data stream. In the case of an odd-parity generator, a parity bit of "1" is added to the data stream to signal that there are an odd number of "1" values present in the transmitted data stream. Fig 5.3 (a) depicts a schematic representation of the PG. A representation of the PG's pNML block diagram is seen in Fig 5.3 (b). Two Ex-OR gates are used in the proposed PG. As seen in Fig. 5.3 (c), all of the inputs are initialised with layer 0. The PG conducts a modulo 2 operation between the three inputs, which are A, B, and C, and between the three outputs. The output of the first Ex-OR gate is fed into the second Ex-OR gate, which in turn feeds into the third Ex-OR gate. The proposed PG employs a total of six mv gates, as seen in Fig. 5.3. (b). To produce the desired outcome, the output Y is reversed. When using pNML technology, the bounding box area of the proposed custom layout of the PG is 21.06 $um^2$, as seen in Fig. 5.3. (c). Fig 5.4 shows the simulation results for the 3D pNML custom architecture of the PG circuit using the pNML. Eq. 5.2 depicts the PG result obtained by the modelling process. Table 5.2 summarises the evaluation of the computational table based on various input combinations to the PG and the results of the evaluation.

Where, $x = M_3\left(1, M_1\left(1, \overline{A}, B\right), M_2\left(1, A, \overline{B}\right)\right)$ ……. (5.2)

$$= \overline{M_3\left(1, \overline{\overline{A} + B}, \overline{A + \overline{B}}\right)}$$

$$= \overline{M_3\left(1, A\overline{B}, \overline{A}B\right)}$$

$$= \overline{\overline{A\overline{B}} + \overline{A}B}$$

$$= A\overline{B} + \overline{A}B = A \oplus B$$

$$Y = \overline{M_6\left(1, M_4\left(1, \overline{X}, C\right), M_5\left(1, \overline{C}, X\right)\right)}$$

$$= \overline{M_6\left(1, \overline{\overline{X} + C}, \overline{\overline{C} + X}\right)} = \overline{M_6\left(1, X\overline{C}, \overline{X}C\right)}$$

$$= \overline{\overline{X\overline{C}} + \overline{X}C} = X\overline{C} + \overline{X}C = A \oplus B \oplus C$$

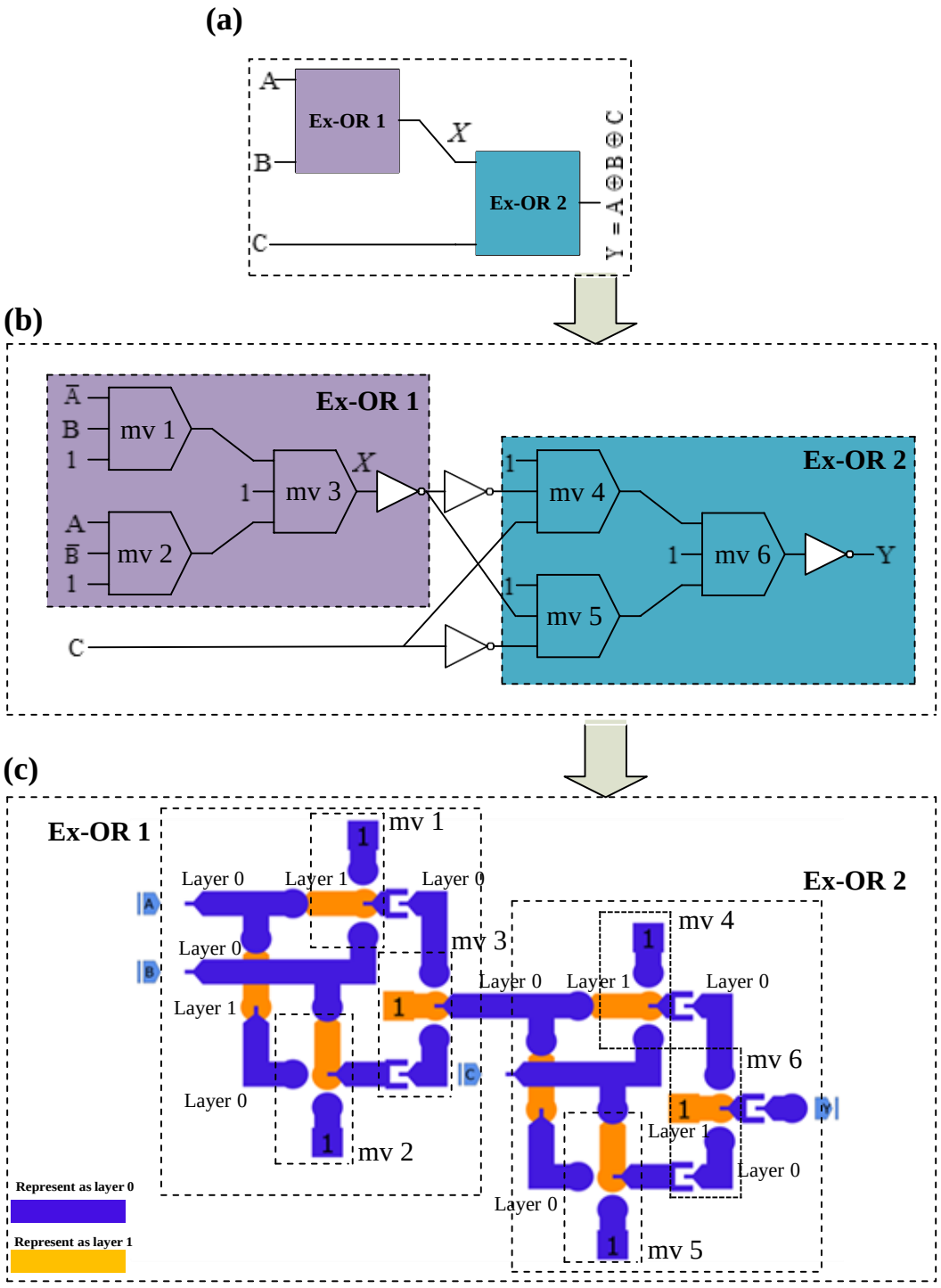



**Fig. 5.3** The proposed PG circuit (a) Schematic (b) pNML block diagram (c) pNML architecture

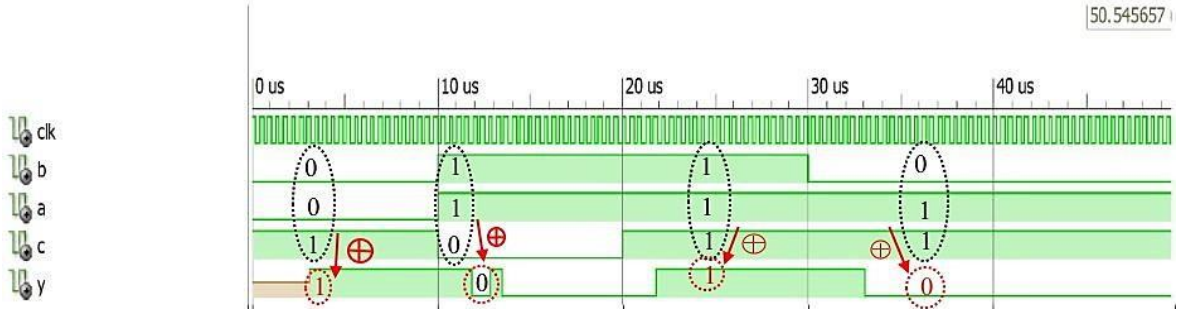



**Fig. 5.4** Simulation result of PG using nano-magnetic pNML

**Table 5.2** Computational Table of PG Circuit with Latency Analysis

| Inputs | | | Output | Latency (in sec) |
|---|---|---|---|---|
| A | B | C | Y | |
| 0 | 0 | 1 | 1 | 5.90 $E^{-6}$ |
| 1 | 1 | 0 | 0 | 3.74 $E^{-6}$ |
| 1 | 1 | 1 | 1 | 3.23 $E^{-6}$ |
| 1 | 0 | 1 | 0 | 6.02 $E^{-6}$ |

## Circuit Design for the Newly introduced Even-Parity Checker in p-NML

A PC is used to identify faults in data transmission at the receiving station. Fig 5.5 (a) is a block diagram of the PC. The number of "1" values in the sent data stream, as well as the parity, are tallied at the receiver's end of the transmission. If the number of "1" values received equals the number of "1" values given, it indicates that there is no mistake in the received data. As shown in Fig. 5.5 (b), the outputs of the first and second Ex-OR gates are sent to the third Ex-OR gate, and the final output is obtained from the third Ex-OR gate. In the example depicted in Fig. 5.5 (c), layer 0 is used to initialise all of the inputs (A, B, C, and P). The PC circuit proprietary layout, which is based on pNML technology, makes use of a total of nine mv gates in its design. Approximately 29.07 $um^2$ is occupied by the bounding box of the suggested model. Fig. 5.6 depicts the simulation results for the 3D pNML circuit for the PC. To assess the model equations that are utilised to synthesise the PC outputs that are based on the mv gates, employ Eqs. 5.3, 5.4, and 5.5. To determine the latency of the suggested PC, four different input combinations are chosen and the simulation is run through. Table 5.3 shows the computation table for the PC.

Intermediate output 1 $X = M_3\left(1, M_1\left(1, \overline{A}, B\right), M_2\left(1, A, \overline{B}\right)\right)$ …… (5.3)

$$= \overline{M_3\left(1, \overline{\overline{A} + B}, \overline{A + \overline{B}}\right)}$$

$$= \overline{M_3\left(1, A\overline{B}, \overline{A}B\right)}$$

$$= \overline{\overline{A\overline{B}} + \overline{\overline{A}B}} = A\overline{B} + \overline{A}B = A \oplus B$$

Intermediate output 2 $Z = \overline{M_6\left(1, M_4\left(1, \overline{C}, P\right), M_5\left(1, C, \overline{P}\right)\right)}$ …….. (5.4)

$$= \overline{M_6\left(1, \overline{\overline{C} + P}, \overline{C + \overline{P}}\right)}$$

$$= \overline{M_6\left(1, C\bar{P}, \bar{C}P\right)}$$

$$= \overline{C\bar{P} + \bar{C}P} = \bar{C}\bar{P} + CP = C \oplus P$$

Final output $Y = \overline{M_9\left(1, M_7\left(1, Z, \bar{X}\right), M_8\left(1, X, \bar{Z}\right)\right)}$ .....(5.5)

$$= \overline{M_9\left(1, \overline{Z + \bar{X}}, \overline{X + \bar{Z}}\right)}$$

$$= \overline{M_9\left(1, \bar{Z}X, Z\bar{X}\right)}$$

$$= \overline{\bar{Z}X + Z\bar{X}} = \bar{Z}\bar{X} + ZX = A \oplus B \oplus C \oplus P$$

**Table 5.3** Computational table of PC circuit

| Input | | | | Output | Latency (in sec) |
|---|---|---|---|---|---|
| A | B | C | P | Y | |
| 0 | 0 | 1 | 0 | 1 | 5.38 $E^{-6}$ |
| 0 | 1 | 0 | 1 | 0 | 4.01 $E^{-6}$ |
| 1 | 0 | 1 | 1 | 1 | 4.14 $E^{-6}$ |
| 1 | 1 | 1 | 1 | 0 | 5.01 $E^{-6}$ |

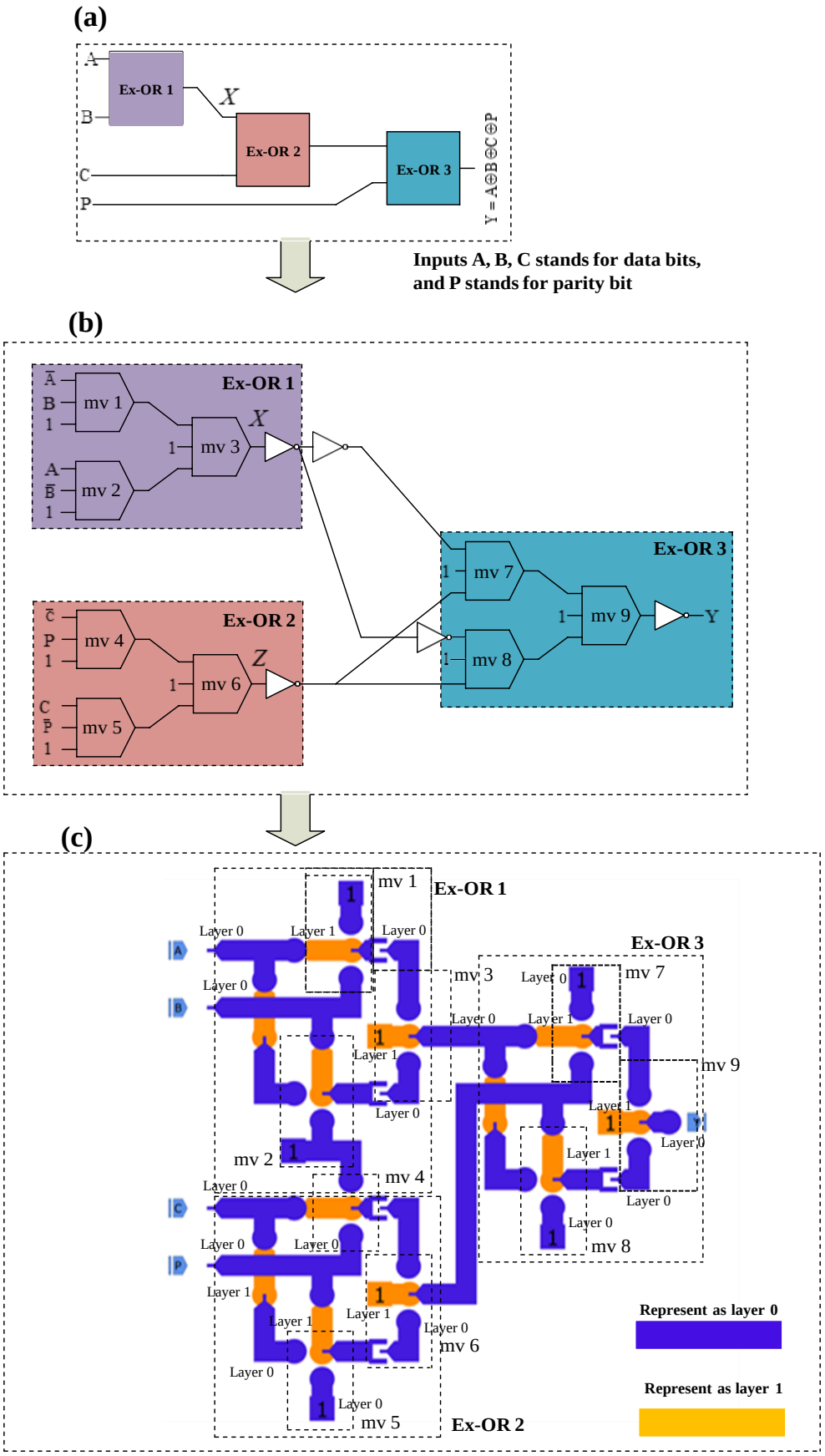



**Fig. 5.5** The proposed PC circuit (a) Block diagram (b) pNML schematic (c) pNML Layout

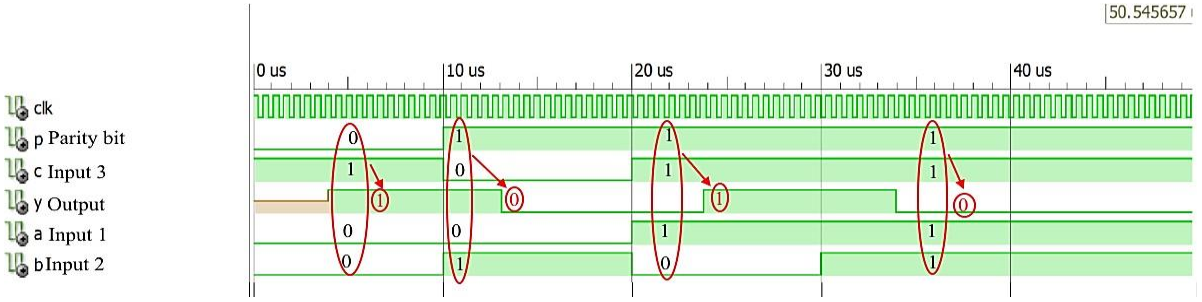



**Fig. 5.6** Simulation result of PC using nano-magnetic pNML

## Results of the PG and PC Circuits in comparison to existing

In this part, the findings for the newly suggested as well as prior PG and PC circuits are discussed in detail. Based on the comparison shown in Table 5.4, the newly suggested pNML-based PG and PC designs outperform the previously proposed PG and PC designs in terms of area, delay (latency), as well as the number of layers, clocks, cells, and magnets used in the designs. Compared to previously published designs as per Bahar et.al. [121], Riente et.al. [124], Hashemi et.al. [125], Angizi et.al. [126], Sheikhfaal, et.al. [127], Singh et.al. [128], Mustafa et.al. [129], Santra et.al. [130], Poorhosseini et.al.[131], the comparison findings show that the new PG and PC are much better.

**Table 5.4** Parameters comparison analysis of Parity generator and checker circuit

| **Existing and Proposed designs** | **Delay (Latency) in Sec** | **Area in μm$^2$** | **Number of magnets or cell count** | **Number of Layer or clock count** | **Single or multilayer** |
|---|---|---|---|---|---|
| Bahar et.al. [121] | 0.75 sec | 0.022 | 24 | 3 clock | Single |
| Hashemi et.al. [125] | 2.75 sec | 0.28 | 168 | 11 clock | Single |
| Angizi et.al. [126] | 2.25 sec | 0.20 | 188 | 8 clock | Single |
| Sheikhfaal, et.al. [127] | 2 sec | 0.11 | 98 | 8 clock | Single |
| Singh et.al. [128] | 1.75 sec | 0.10 | 87 | 6 clock | Single |
| Mustafa et.al. [129] | 2 sec | 0.17 | 99 | 8 clock | Single |
| Santra et.al. [130] | 2 sec | 0.053 | 60 | 8 clock | Single |
| Poorhosseini et.al. [131] | 2 sec | 0.08 | 82 | 7 clock | Single |
| Das et.al. [132] | 1.75 sec | 0.05 | 54 | 7 clock | Single |
| Newly PG | 6.02 μsec | 21.06 | 28 | 2 layer | Multilayer |
| Newly PC | 5.38 μsec | 29.07 | 39 | 2 layer | Multilayer |
| Improvement of PG in % Poorhosseini et.al. [131] | - | NI | 65.85 | 71.42 | - |
| Improvement of PG in % Das et.al. [132] | - | NI | 48.14 | 71.42 | - |
| Improvement of PC in % Mustafa et.al. [129] | - | NI | 66.66 | 77.77 | - |
| Improvement of PC in % Das et.al. [132] | - | NI | 27.77 | 71.42 | - |

The comprehensive evaluation of both the new and prior PG and PC designs are presented in Table 5.4. In contrast to Refs. Mustafa et.al. [129], Santra et.al. [130], Poorhosseini et.al. [131], the new design for the PG achieves improvements of 65.85 percent, 48.14 percent, and 71.42 percent in terms of the number of magnets or cells, the number of layers, and the number of clocks counts, respectively, compared to the previous design. Comparing the new design described here with the reference PC design reported in Mustafa et.al. [129], Poorhosseini et.al. [131], the new design provides improvements in the number of magnets or cells, the number of layers, the number of clock counts, and the number of layers or clock counts of 66.66 percent, 27.77 percent, 77.77 percent, and 71.42 percent, respectively.

The new design for the PG and PC in pNML uses fewer magnets and layers, resulting in lower latency and less power consumption. Furthermore, both the PG and PC designs that have been presented are built on multilayer pNML technology. Because of these low-cost designs for PG and PC circuits, there are more application options for sophisticated, high-density, and high-speed computing nano-circuits than ever before.

**The Proposed Multiplexer in p-NML Technology**

Multiplexers are devices that have $2^n$ input lines and one or more selected lines. The two inputs (A and B) and the single select line (SEL) of a 2-to-1 mux is seen in Fig. 5.7 (a). Selecting which of the inputs is to be transferred to the output line is accomplished via the use of the SEL command. A layer "0" is assigned to all of the inputs A, B, and SEL; the first mv1 receives A as input, as well as SEL's invoicing information and a fixed value of zero. B, SEL, and a fixed "0" are provided as input to mv2. As demonstrated in Fig. 5.7 (b), the output of both mv gates is passed to mv3, which yields the required output. The suggested model has a bounding box with a surface size of 13.5 $\mu m^2$. The new mux is composed of two layers (layer 0 and layer 1), both of which are based on magnets. As shown in Fig 5.7 (c), the 2:1 mux in pNML technology is developed in this manner. The results of the simulation are shown in Fig. 5.8. If the input SEL combination is 0, the correct output combination of Y = A is obtained, as illustrated in Fig. 5.8. If the input SEL combination is 1, the accurate output combination of Y = B is found in Eq. 5.6, where A, B, and SEL are the inputs and Y is the output of a 2:1 mux, is used to calculate the output of the 2:1 mux. Table 5.5 shows the latency for the proposed 2:1 mux created in pNML technology, as well as the delay for other 2:1 mux designs.

$$\text{Output } Y = M_3\left(0, M_1\left(0, A, \overline{SEL}\right), M_2(0, SEL, B)\right) \quad \text{..... (5.6)}$$

$$= M3\left(0, \overline{A.\overline{SEL}}, \overline{B.SEL}\right)$$

$$= \overline{\overline{A.\overline{SEL}}}\,\overline{\overline{B.SEL}}$$

$$= \overline{\overline{A.\overline{SEL}}} + \overline{\overline{B.SEL}}$$

$$= A.\overline{SEL} + B.SEL$$

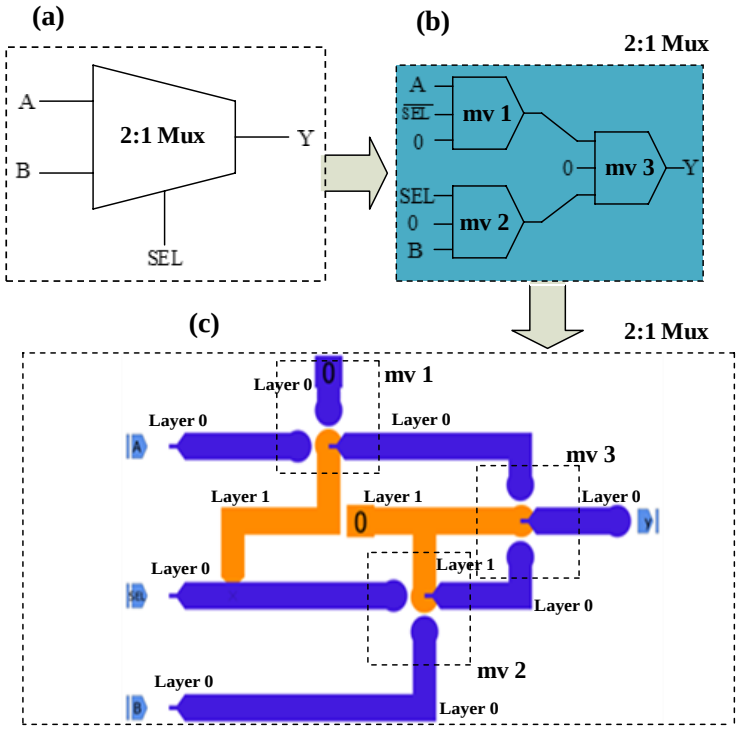



**Fig. 5.7** The proposed 2:1 mux circuit (a) Block diagram (b) pNML schematic (c) pNML Layout.

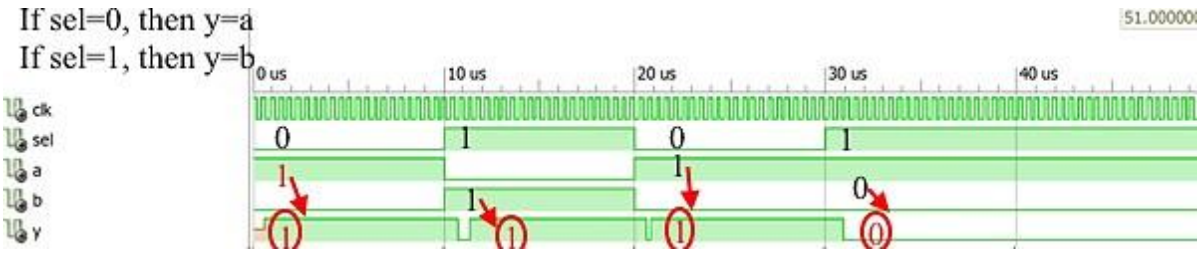



**Fig. 5.8** Simulation result of 2:1 mux using nano-magnetic pNML

**Table 5.5** Computational table of 2 to 1 multiplexer

| Input | | | Output (Y) | Latency (in sec) |
|---|---|---|---|---|
| SEL | A | B | | |
| 0 | 0 | 0 | 0 | $0.73E^{-6}$ |
| 0 | 0 | 1 | 0 | $0.84\ E^{-6}$ |
| 0 | 1 | 0 | 1 | $0.58\ E^{-6}$ |
| 0 | 1 | 1 | 1 | $0.97\ E^{-6}$ |
| 1 | 0 | 0 | 0 | $1.18\ E^{-6}$ |
| 1 | 0 | 1 | 1 | $1.38\ E^{-6}$ |
| 1 | 1 | 0 | 0 | $0.96\ E^{-6}$ |
| 1 | 1 | 1 | 1 | $1.48\ E^{-6}$ |

## The pNML technology 4:1 multiplexer architecture

A 4:1 mux is made up of a pair of 2:1 muxes connected. As seen in Fig. 5.9 (a), it contains four input lines (a, b, c, and d) and two select lines (s0 and s1) in addition to the output lines. In Table 5.6, the truth table for a 4 to 1 mux is shown, with s0 and s1 representing the select lines; the input lines (a, b, c, d) representing the input lines; and the output line representing by y. When constructing the desired output of a 4:1 mux, the inputs a, b, c, and s0 and s1 are initialised with layer zero, while input d is initialised with layer one. The inverted input is then applied in all situations to get the multiplexer output Eq. 5.7. Based on the mv and inverter of the new 4:1 mux, a schematic is shown in Fig. 5.9 (b), and the layout in pNML design is presented in Fig. 5.9 (c), respectively. Approximately 25.65 $um^2$ is occupied by the bounding box of the suggested model. According to Fig. 5.10, the simulation results of a 4:1 mux architecture with four inputs, two numbers of select lines, and one output were obtained. Modelling the output of a 4:1 mux is accomplished using equation 5.7. From the simulation of the suggested architecture, to calculate the latency for various combinations of inputs are demonstrated in Table 5.7.

$$Y = M_{11}\left(0, M_5\left(1, M_2\left(1, \bar{a}, \overline{s0.s1}\right), M_4\left(1, \bar{b}, \overline{s0.s1}\right)\right), M_{10}\left(1, M_7\left(1, \bar{c}, \overline{s0.s1}\right), M_9\left(1, \bar{d}, \overline{s0.s1}\right)\right)\right) \quad \text{-- (5.7)}$$

$$= M_{11}\left(0, M_5\left(1, \underline{a} + \underline{s0.s1}, \underline{b} + \underline{s0.s1}\right), M_{10}\left(1, \underline{c} + \underline{s0.s1}, \underline{d} + \underline{s0.s1}\right)\right)$$

$$= M_{11}\left(0, M_5\left(1, a.\bar{s0}.s1, b.\bar{s0}.\bar{s1}\right), M_{10}\left(1, c.s0.\bar{s1}, d.s0.s1\right)\right)$$

$$= M_{11}\left(0, \overline{a.\bar{s0}.s1 + b.\bar{s0}.\bar{s1}}, \overline{c.s0.\bar{s1} + d.s0.s1}\right)$$

$$= \overline{\left(a.\bar{s0}.s1 + b.\bar{s0}.\bar{s1}\right).\left(c.s0.\bar{s1} + d.s0.s1\right)}$$

$$= a.\bar{s0}.s1 + b.\bar{s0}.\bar{s1} + c.s0.\bar{s1} + d.s0.s1$$

**Table 5.6.** Truth table of 4 to 1 multiplexer

| S0 | S1 | d | c | b | a | Y |
|---|---|---|---|---|---|---|
| 0 | 0 | x | x | x | 1 | 1 |
| 0 | 1 | x | x | 1 | x | 1 |
| 1 | 0 | x | 1 | x | x | 1 |
| 1 | 1 | 1 | x | x | x | 1 |

**Table 5.7.** Computational analysis of 3D pNML layout of 4 to 1 multiplexer

| Inputs | | | | | | Output (Y) | Latency(in sec) |
|---|---|---|---|---|---|---|---|
| S0 | S1 | a | b | c | d | | |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 2.73 $E^{-6}$ |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 2.86 $E^{-6}$ |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 2.33 $E^{-6}$ |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1.58 $E^{-6}$ |

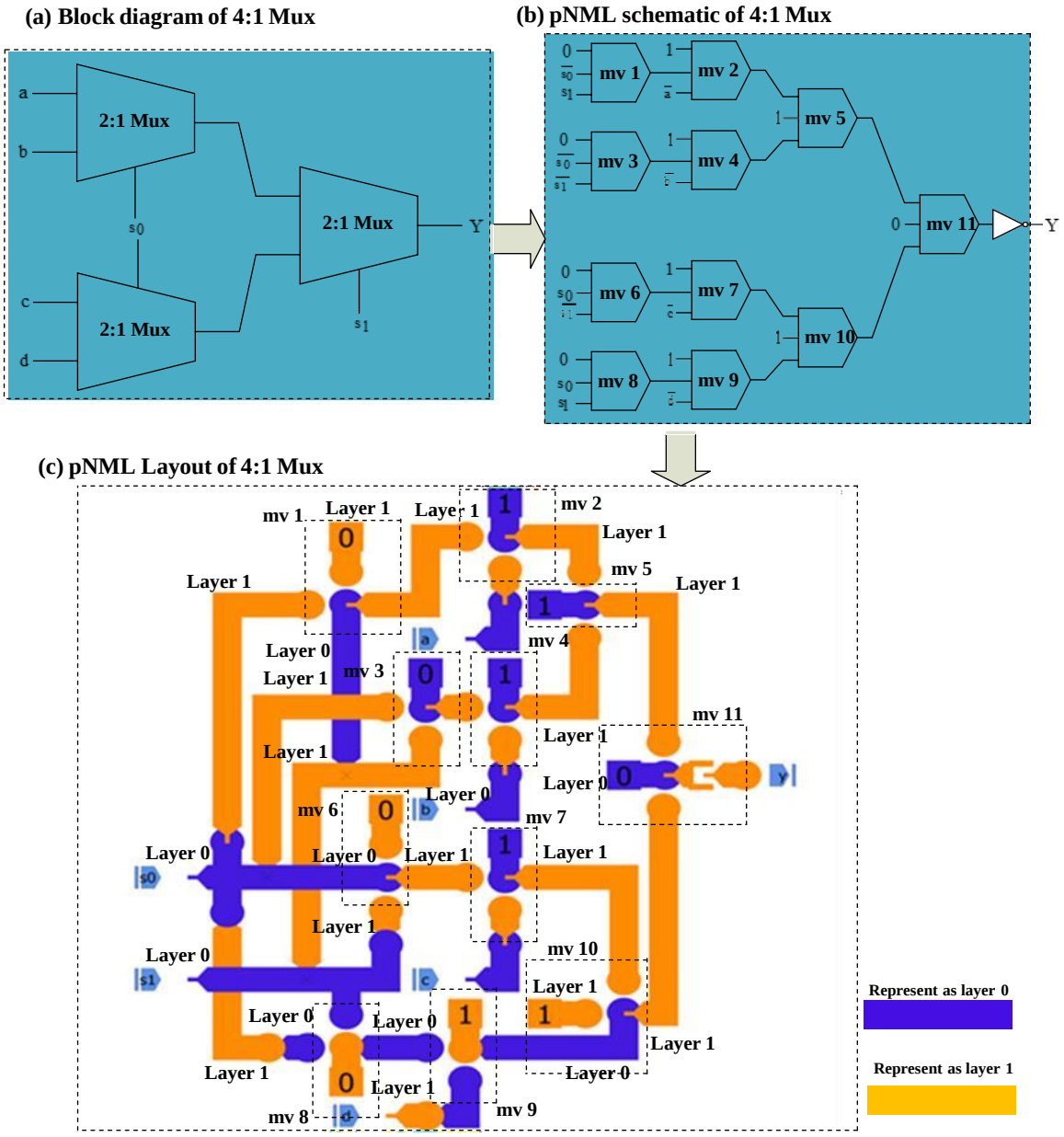



**Fig. 5.9** The proposed 4:1 mux circuit (a) Block diagram (b) pNML schematic (c) pNML Layout

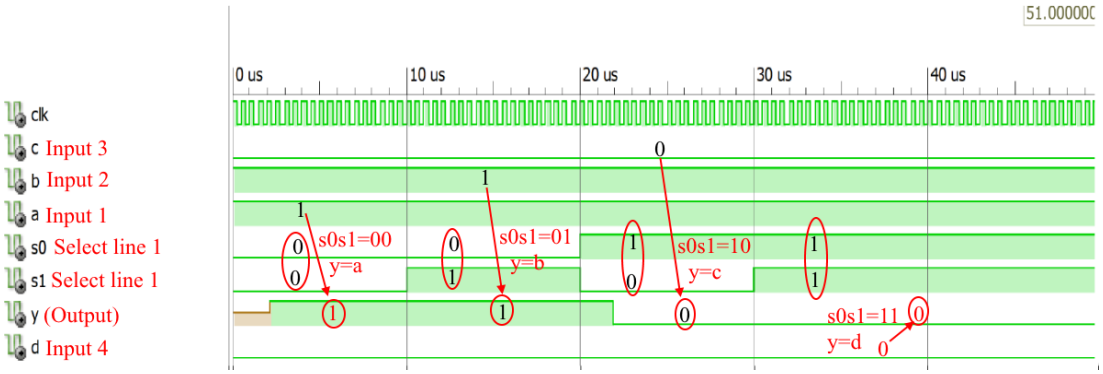



**Fig. 5.10** Simulation result of 4 to 1 mux using nano magnetic pNML

## Comparative results of multiplexer circuits

Numerous papers on QCA circuits have been published in the scientific literature, demonstrating its effectiveness. The downside of QCA technology has been its inability to work at room temperature, while magnetic circuits, on the other hand, may have a physical implementation that is achievable at any temperature in Erniyazov et.al. [119]. According to the current study, magnetic circuits are in high demand because they can be developed in 3D layout and because they are a very fast switching speed in Riente et.al. [120]. This is because they can be designed in a 3D layout and because they are extremely fast. The suggested mux designs that are presented are quite compact, and the latency value that is reported here is very low, as previously stated. According to the results of the comparative analysis in Table 5.8, the new mux design based on pNML is superior to the literature work in Ahmad et.al. [123], Kim et.al. [133], Amiri et.al. [135], Mardiris et.al. [134], Oskouei et.al. [136]. The suggested mux, which is based on low-cost parameters, will be ideal for sophisticated ALU and processor architectures. The suggested 2:1 mux and 4:1 mux are also synthesised in multilayers with the use of magnets, which is another advantage.

**Table 5.8** Comparison of new multiplexer design with literature designs

| **Existing and Proposed designs** | **Delay (Latency)** | **Area in μm$^2$** | **Number of magnets or cell count** | **Number of Layer or clock count** | **Single or multilayer** |
|---|---|---|---|---|---|
| Ahmad et.al. [123] in 2:1 mux design | 2 sec | 0.01 | 16 | 2 clock | Single |
| Kim et.al. [133] in 2:1 mux design | 4 sec | 0.08 | 41 | 2 clock | Single |
| Amiri et.al. [135] in 2:1 mux design | 4 sec | 0.03353 | 34 | 3 clock | Single |
| Mardiris et.al. [134] in 2:1 mux design | 11 sec | 0.67 | 633 | 7 clock | Single |
| Oskouei et.al. [136] in 4:1 mux design | - | - | 143 | 8 clock | Single |
| Newly 2:1 mux design | 2.01 μs | 13.5 | 9 | 2 layer | Multilayer |
| Newly 4:1 mux design | 2.88 μs | 25.65 | | 2 layer | Multilayer |
| Improvement of 2:1 mux in % as per Amiri et.al. [135] | VH | NI | 73.52 | 33.33 | - |
| Improvement of 2:1 mux in % as per Mardiris et.al. [134] | VH | NI | 98.57 | 71.42 | - |
| Improvement of 4:1 mux in % as per Oskouei et.al. [136] | VH | NI | | 75 | - |

VH-Very high, NI-No improvement

**The proposed 3D layout of ALU**

Fig 5.11 (a) depicts a schematic representation of the ALU. The circuit is made up of the following modules: HA, OR, Ex-NOR, and AND gates, among others. The inputs are received by all of the modules (r, s). One 2:1 mux is used to carry out the different procedures. The select lines (s0 and s1) utilised in the mux design are responsible for executing the different combinations, such as Ex-OR, OR, NOR, and AND, among others. When the input operands include the rs='01' prefix, the selected value of the mux will be

fixed as s0s1=00, and the mux will perform Ex-OR operations on the input. Table 5.9 shows the results of evaluating and drawing the calculation table for various input combinations of r and s. In Fig. 5.11 (b) schematic representation of an ALU that is based on the mv gate and inverter. Fig 5.11(c) depicts a diagrammatic representation of the planned ALU's overall layout. The mv gates (mv12, mn13, mn15, and mn16) received the inputs as r and s, and when intermediate outputs are processed by mv gates, the final outputs are received as r and s as well (mv1 to mn10). Furthermore, the outputs are acquired by the use of mv 11. The output node y is determined by the input r and s combinations, and the final ALU outputs are acquired from the output node y. In Fig. 5.11 (b), the block-level schematic has been used by 17 mV and 6 inverters to design their circuits. It is possible to conduct numerous ALU operations using the MagCAD tool by using the suggested architecture of ALU that is based on the mv, and inverter gate. The 3D configuration of the proposed ALU is shown in Fig. 5.11. (c). A variety of logic gates are linked in this circuit instead of the four inputs of the multiplexer labelled "a," "b," "c," and "d." The input to all of the logic gates is provided by the variables 'p' and 'q', which are initialised with a layer '0,' whilst the output 'y' is obtained by taking use of the variable 'y'. Select lines s1 and inversion of s0 are linked to the sum result of the half adder, which is transmitted to the output line 'y' when the input 'a' is connected to the half adder's sum result. The carry result of a half adder is produced by the function 'p'. When the select line invert of s0 and the select line invert of s1 are chosen, the input 'b' is linked to the 'OR' gate and is transferred to the output line. Additionally, inputs c and d are linked to the "EXNOR" and "AND" gates, respectively, in a similar fashion. The select lines for the Ex-NOR gate are s0 and the invert of s1, and the select lines for the AND gate are s0 and s1. The select lines for the AND gate are s0 and s1. The suggested model has a bounding box area of 58.59um$^2$, which is a little amount of space. Modelsim v10 is used to model the ALU architecture that has been presented. Figure 5.12 shows four different variations of the simulation findings. All of the test results demonstrate that the ALU's logic circuits are operating correctly. The latency value has been calculated based on the different input combinations and is provided in Table 5.9. Below is shown the model equation for the suggested ALU, which is based on the pNML architecture, as seen in the equation.

$$y = M_{11}\left(\begin{array}{l} M_5\left(1, M_2\left(1, \bar{a}, M_1\left(0, \bar{s}0, s1\right)\right), M_4\left(1, \bar{b}, M_3\left(0, \bar{s}0, \bar{s}1\right)\right)\right), 0, \\ M_{10}\left(M_7\left(1, \bar{c}, M_6\left(0, s0, \bar{s}1\right)\right), 1, M_9\left(1, \bar{d}, M_8\left(0, s1.s0\right)\right)\right) \end{array}\right)$$

Where $a = \overline{M_{12}\left(1, \bar{r}s, r\bar{s}\right)}$

$$= \overline{\bar{r}s + r\bar{s}}$$

$$= \bar{r}s + r\bar{s}$$ **(Ex-OR GATE)**

$$b = \overline{M_{15}\left(r, 1, s\right)}$$

$$= \overline{r + s}$$

$$= r + s$$ **(OR GATE)**

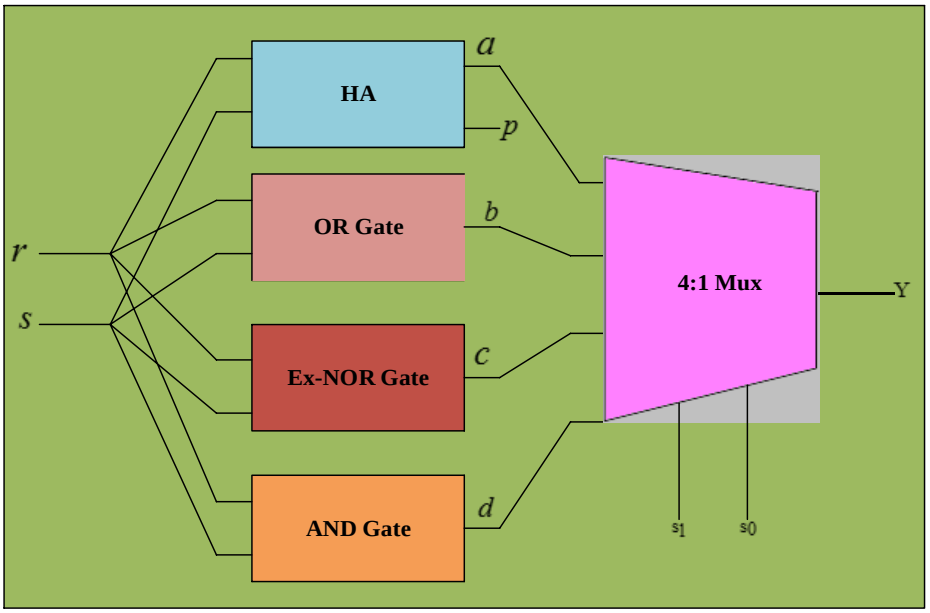
$$c = M_{14}\left(1, \bar{r}s, r\bar{s}\right)$$

$= \overline{\overline{rs} + \overline{rs}}$ **(Ex-NOR GATE)**

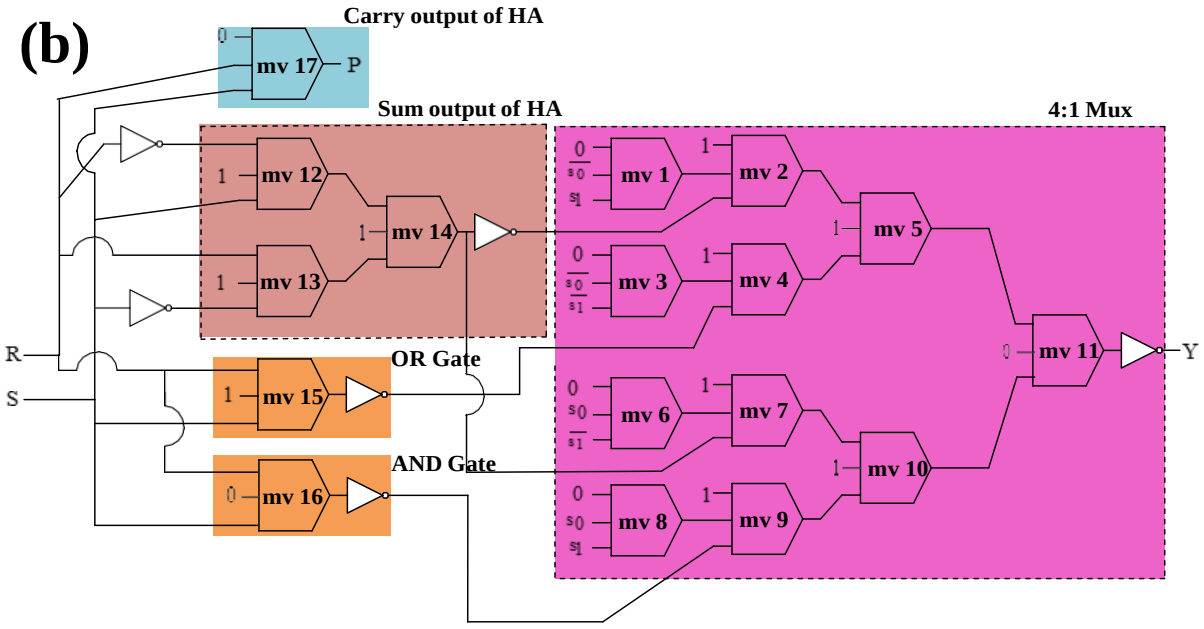
$d = \overline{M_{16}(r,0,s)}$

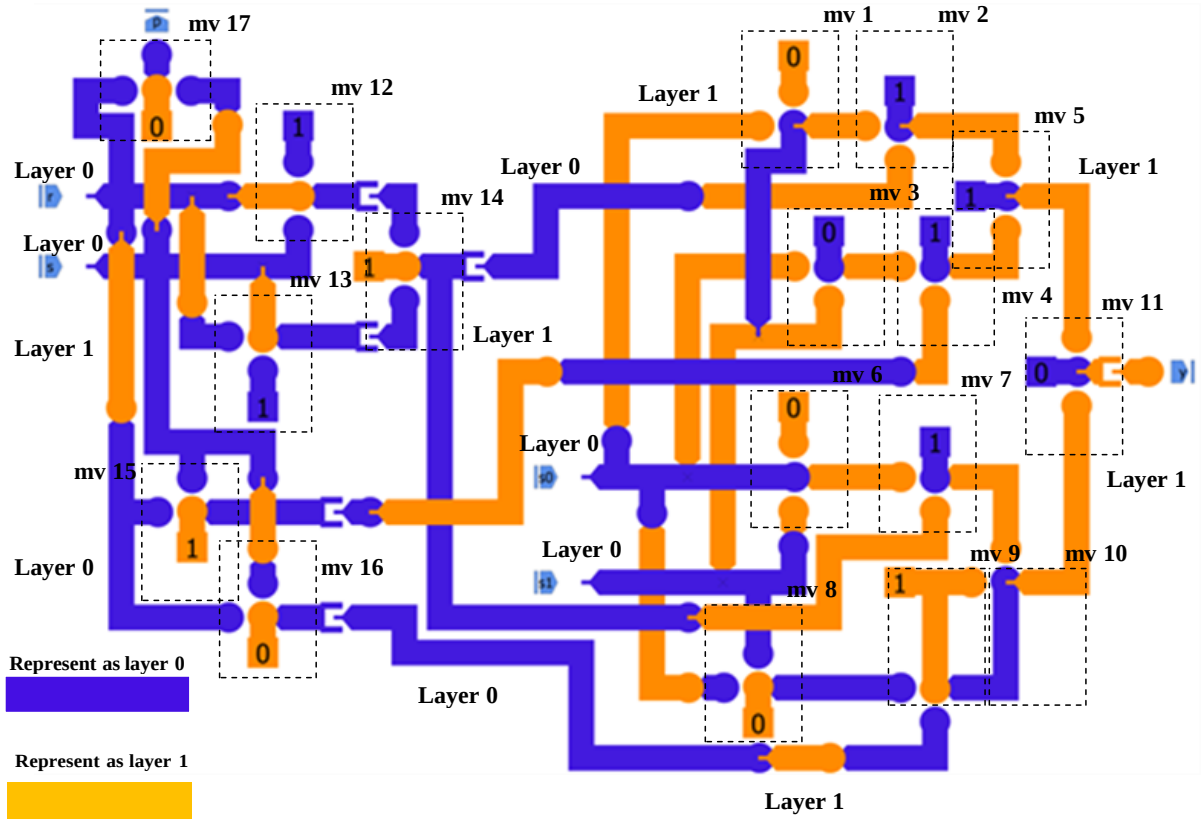
$= \overline{\overline{r.s}} = r.s$ **(AND GATE)**

**(a)**




**(b)**






(c)

**Fig 5.11**. The proposed ALU circuit (a) Block diagram (b) pNML schematic (c) pNML Layout

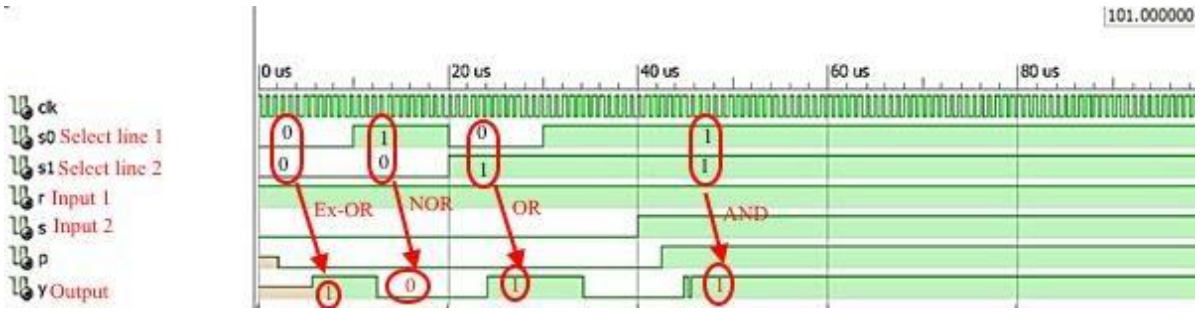



**Fig. 5.12** Simulation result of ALU using nano-magnetic pNML technology

**Table 5.9** Computational table of ALU

| Inputs | | | | Output | Latency | ALU operations |
|---|---|---|---|---|---|---|
| **s0** | **s1** | **r** | **s** | **y** | | |
| 0 | 0 | 0 | 1 | 1 | 3.88 $E^{-6}$ | Ex-OR |
| 0 | 1 | 0 | 1 | 1 | 2.53$E^{-6}$ | OR |
| 1 | 0 | 1 | 0 | 0 | 2.32 $E^{-6}$ | NOR |
| 1 | 1 | 1 | 1 | 1 | 2.63 $E^{-6}$ | AND |

### 5.1.9 Comparative results of ALU circuits

In pNML technology, the synthesis of layout is critical for the design of ALU circuits. In contrast to current literature, the compact ALU suggested here is based on NML logic and performs better in terms of latency, number of magnets or cell count, number of clocks, and layer count than the existing literature. When comparing the proposed ALU design based on pNML to current designs Oskouei et.al. [136], Ghosh et.al. [137], Sen et.al. [138], Goswami et.al. [139], Gadim et.al. [140], the findings are shown in Table 5.10 demonstrate that the proposed ALU design based on pNML gives the lowest value of latency, magnet or cell count, and clock or layer count. In the literature, there are no designs based on pNML, however, there are more designs based on QCA that may be used for the comparative study of the ALU. It has a lower latency value and a higher number of clocks or layer count than the previous designs, which may be attributed to the several layers of the ALU architecture. According to Oskouei et.al. [136], Ghosh et.al. [137], Sen et.al. [138], Goswami et.al. [139], Gadim et.al. [140], when compared to the QCA-based ALU, the performance characteristics such as layer count, the magnet utilised, and latency are stated to be superior in Oskouei et.al. [136], Ghosh et.al. [137], Sen et.al. [138], Goswami et.al. [139], Gadim et.al. [140] Because of the improved ALU, there is a reduced cost in terms of parametric analysis, which includes factors such as layer count, magnet utilised, and latency. According to Sen et.al. [138], Goswami et.al. [139], Gadim et.al. [140], the newly developed ALU utilises 97.13 percent, 93.63 percent, and 85.34 percent fewer magnets and cell count than the previously developed designs. When compared to conventional literature, the low-cost factors shown in the above study are the most significant.

**Table 5.10** Comparative analysis results of ALU

| **Existing and Proposed designs** | **Delay (Latency)** | **Area in $\mu m^2$** | **Number of magnets or cell count** | **Number of clock or Layer count** | **Single or multilayer** |
|---|---|---|---|---|---|
| Oskouei et.al. [136] | 3 | 0.38 | 332 | 3 clock | Single |
| Ghosh et.al. [137] | 5 | 0.79 | 485 | 9 clock | Single |
| Sen et.al. [138] | 6 | 4.01 | 2370 | - | Single |
| Goswami et.al. [139] | 2 | 2.34 | 1069 | 9 clock | Single |
| Gadim et.al. [140] | 3 | 0.78 | 464 | 11 clock | Single |
| New ALU design | 3.88µsec | 58.59 | 68 | 2 layer | Multilayer |
| % Improvement w.r.to ref. Sen et.al. [138] | VH | NI | 97.13 | - | - |
| % Improvement w.r.to ref. Goswami et.al.[139] | VH | NI | 93.63 | 77.77 | - |
| % Improvement w.r.to ref. Gadim et.al. [140] | VH | NI | 85.34 | 81.81 | - |

## CONCLUSION REMARKS

Exploring various new digital circuits in pNML is designed in this chapter.

The major achievement of this chapter are highlighted below:

**1** The introduction of two input Ex-Or is being proposed to reduce the minority gate count in pNML-based circuits such as PG, PC, mux and ALU. The MagCAD 2.10.0 programme was used to create circuits such as Ex-Or, PG, PC, mux, and ALU to evaluate the newly created digital circuit architecture.

**2** The extracted parameters such as bounding box area, layer count, and latency are presented for all the proposed circuits. Simulation results based on the external simulator of Modelsim v10.4 version showed that a significant amount of latency was reduced without much alter over the critical path. To make the designed circuits more robust and less latency for all the combinations, which offer a great benefit in designing efficient combinational circuits. Comparison results show that proposed circuits perform better compared to state-of-the-art ones.

# CHAPTER 6

# CONCLUSION AND FUTURE WORK

Power loss and fast switching are becoming more important problems in current nano-scale CMOS logic circuits, and they have become a fundamental challenge. Technology such as reversible logic, on the other hand, offers a solution for managing the information erasure in logic circuits, and it may also be a viable answer for power reduction in coming technologies like advanced computing systems. It also serves as a fundamental building block for the creation of quantum computers, since quantum circuits are based on the reversible logic gate. When it comes to nano-scale computing standards, the most notable stumbling block is the enormous waste of power. By computing using reversible gates in the quantum circuit, it is possible to achieve extremely low power dissipation. It is possible to achieve reversibility in a certain logic circuit by leveraging phenomena of bijective character between nodes of the input and output lines. This dissertation deal with conservative reversible logic based multiplexer design.

Emerging QCA technology has shown to be an acceptable alternative to MOS technology for a nano-circuit design that requires high device density, while also requiring low power. As a result, in this dissertation work, a novel structure of QCA technology-based nano-circuits, such as CAM memory and reversible multiplexer, are built using this technology.

Digital circuits need to be increased switching speed, a less complicated design, and reduced energy consumption to function properly. The utilisation of advanced computing technologies, such as NML, for nano-circuit design at high switching speeds, has resulted in the development of a viable alternative for MOS-based VLSI applications. As a result of its capacity to process logic bits as well as store logic bits in a single device, nano-scale based NML technology has significant promise as a platform for advanced computing applications. Since NML technology is rapidly approaching its smallest feature size, high device density, and ability to work at room temperature, it is becoming more popular. This dissertation deal with NML based parity generator, parity checker and ALU design.

This dissertation is concerned with the synthesis, optimization, and verification of the circuits, quantum circuit synthesis, and logic based on quantum-dot cellular automata, as well as their applications. This dissertation study is summarised into six chapters, which also includes potential future work that might be done in the future.

The unique contribution, various cost-efficient nano-circuit are designed for energy-aware sustainable computing. The suggested designs have seen less significant delay, and less footprint area demonstrating the effectiveness of the design synthesis technique.

In Chapter 3, the first contribution, the technique, which is based on an expanded viewpoint, frames the multiplexer modules that have been suggested. Furthermore, the quantum cost and gate count are kept to a minimum to maintain an effective quantum computing framework. The QCA computing framework, in addition, is an effort to synthesise the optimum primitives in a conservative reversible multiplexer for use in a Nano-electronic confined application. The lemma that has been created is framed to demonstrate the optimum parameters in the reversible circuit. Concerning currently available advanced technologies, the suggested modular multiplexer's gate count, quantum cost, and unit latency are the most efficient available.

It is described in this chapter 4 as the first contribution, how to synthesise the CAM memory in the context of nano-technology using a matching and memory unit. The designed CAM circuit has a small number of cells (33 total) and a small number of majority gates (6 total). Furthermore, the clock cycle delay of the CAM cell design is less than or equivalent to the other stated values, resulting in a circuit with a low delay as a consequence of the reduced delay. A smaller propagation delay is desired as it would enable high speed. The crucial feature of polarisation variation is discussed in detail utilising a QCA arrangement in conjunction with temperature. The second contribution, in chapter 4, the pNML technology is used to optimise the architecture of CAM memory. One of the primary goals of this implementation is to synthesise CAM memory concerning latency and various other design parameters. The design is implemented using a multilayer technique, which is the most efficient method. In terms of layout building of designs, the synthesis technique and optimization are great scalability candidates. It is believed that the first time a memory unit and a matching unit in the pNML are combined to synthesise design in a high-speed pNML application is being presented in the state-of-the-art.

In Chapter 5, the main contribution demonstrated as nano-magnetic logic is resistant to radiation; it functions as non-volatile memory and exhibits zero leakage current, which is essential for high-speed and low-cost nano-electronics applications that need low-cost and high-speed logic. In this study, pNML technology is used to synthesise unique and structured designs such as 3D Ex-OR, PG, PC, multiplexer, and arithmetic-logic-unit (ALU). The previous designs, when measured in terms of latency, layer count, and bounded-area, are not compact. It has been recommended that new designs such as the Ex-OR, PG, PC, multiplexer, and ALU employing pNML be used to address this problem, since they use less space and have lower latency than preceding circuits. The newly ALU consumes 93.63% less than the number of magnets or cell count consumed by previous designs in the literature.

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